APPLICATION FOR UNITED STATES LETTERS PATENT

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TITLE: PILOT SIGNALS FOR SYNCHRONIZATION AND/OR CHANNEL ESTIMATION

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PILOT SIGNALS FOR SYNCHRONIZATION AND/OR CHANNEL ESTIMATION

This application claims the benefit of U.S. Provisional Application No. 60/136,763 filed May 28,1999, and this application is also a continuation-in-part of Application No. _____ filed August 13, 1999, whose entire disclosure is incorporated herein by reference therein.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to communication systems, and more particularly, wireless communication systems, preferably, wide band code division multiple access (W-CDMA) communication systems.

2. Background of the Related Art

The use of code division multiple access (CDMA) modulation techniques is one of several techniques for facilitating communications in which a large number of systems are present. Figure 1 generally illustrates a system 10, which uses CDMA modulation techniques in communication between user equipment (UE) 12a and 12b, each UE including a cellular telephone, and base stations (BTS) 14a and 14b. A base station controller (BSC) 16 typically includes an interface and processing circuitry for providing system control to the BTS 14a, 14b. The BSC 16 controls the routing of telephone calls

from the public switched telephone network (PSTN) to the appropriate BTS for transmission to the appropriate UE. The BSC 16 also controls the routing of calls from the UEs, via at least one BTS to the PSTN. The BSC 16 may direct calls between UEs via the appropriate BTS since UEs do not typically communicate directly with one another. The BSC 16 may be coupled to the BTS 14a and 14b by various means including dedicated telephone lines, optical fiber links or by microwave communication links.

The arrows 13a-13d define the possible communication links between the BTS 14a and UEs 12a and 12b. The arrows 15a-15d define the possible communication links between the BTS 14ba and UEs 12a and 12b. In the reverse channel or uplink (i.e., from UE to BTS), the UE signals is received by BTS 14a and/or BTS 14b, which, after demodulation and combining, pass the signal forward to the combining point, typically to the BSC 16. In the forward channel or downlink (i.e., from BTS to UE), the BTS signals are received by UE 12a and/or UE 12b. The above system is described in U.S. Patent Nos. 5,101,501; 5,103,459; 5,109,390; and 5,416,797, whose entire disclosure is hereby incorporated by reference therein.

A radio channel is a generally hostile medium in nature. It is rather difficult to predict its behavior. Traditionally, the radio channels are modeled in a statistical way using real propagation measurement data. In general, the signal fading in a radio environment can be decomposed into a large-scale path loss component together with a medium-scale slow varying component having a log-normal distribution, and a small-scale

fast varying component with a Rician or Rayleigh distribution, depending on the presence or absence of the line-of-sight (LOS) situation between the transmitter and the receiver.

Figure 2 illustrates these three different propagation phenomena. An extreme variation in the transmission path between the transmitter and receiver can be found, ranging from direct LOS to severely obstructed paths due to buildings, mountains, or foliage. The phenomenon of decreasing received power with distance due to reflection, diffraction around structures, and refraction is known as path loss.

As shown, the transmitted signal is reflected by many obstacles between a transmitter and a receiver, thus creating a multipath channel. Due to the interference among many multipaths with different time delays, the received signal suffers from frequency selective multipath fading. For example, when the 2GHz carrier frequency band is used and a car having a UE is travelling at a speed of 100km/h, the maximum Doppler frequency of fading is 185Hz. While coherent detection can be used to increase link capacity, under such fast fading, the channel estimation for coherent detection is generally very difficult to achieve. Because of fading channels, it is hard to obtain a phase reference for the coherent detection of data modulated signal. Therefore, it is beneficial to have a separate pilot channel.

Typically, a channel estimate for coherent detection is obtained from a common pilot channel. However, a common pilot channel transmitted with an omnidirectional antenna experiences a different radio channel than a traffic channel signal transmitted

through a narrow beam. It has been noticed that common control channels are often problematic in the downlink when adaptive antennas are used. The problem can be circumvented by user dedicated pilot symbols, which are used as a reference signal for the channel estimation. The dedicated pilot symbols can either be time or code multiplexed.

Figure 3 depicts a block diagram of a transmitter and a receiver for time multiplexed pilot symbols for an improved channel estimation method that works satisfactorily under slow-to-fast fading environments. Known pilot symbols are periodically multiplexed with the sequence of the transmitted data. The pilot symbols and data symbols following pilot symbols constitute a slot, as shown in Figure 3.

Further, in a DS-CDMA transmitter, the information signal is modulated by a spreading code, and in the receiver, it is correlated with a replica of the same code. Thus, low cross-correlation between the desired and interfering users is important to suppress the multiple access interference. Good autocorrelation properties are required for reliable initial synchronization, since large sidelobes of the autocorrelation function may lead to erroneous code synchronization decisions. Furthermore, good autocorrelation properties are important to reliably separate the multipath components.

Since the autocorrelation function of a spreading code should resemble, as much as possible, the autocorrelation function of white Gaussian noise, the DS code sequences are also called pseudo-noise (PN) sequences. The autocorrelation and cross-correlation functions are connected in such a way that it is not possible to achieve good

autocorrelation and cross-correlation values simultaneously. This can be intuitively explained by noting that having good autocorrelation properties is also an indication of good randomness of a sequence. Random codes exhibit worse cross-correlation properties than deterministic codes.

Such mobile communication system has gone through different stages of evolution, and various countries used different standards. First generation mobile systems in the 1980s used analog transmission for speech services. Advanced Mobile Phone Service (AMPS) in the United States, Total Access Communication System (TACS) in the United Kingdom, Nordic Mobile Telephones (NMT) in Scandinavia, Nippon Telephone and Telegraph (NTT) in Japan, etc., belonged to the first generation.

Second generation systems using digital transmission were introduced in the late 1980s. They offer higher spectrum efficiency, better data services, and more advanced roaming than the first generation systems. Global System for Mobile Communications (GSM) in Europe, Personal Digital Cellular (PDC) in Japan, and IS-95 in the United States belonged to the second generation.

Recently, third generation mobile radio networks have been under intense research and discussion and will emerge around the year 2000. In the International Telecommunication Union (ITU), the third generation networks are called International Mobile Telecommunications - 2000 (IMT-2000) and in Europe, Universal Mobile

Telecommunication System (UMTS). IMT-2000 will provide a multitude of services, including multimedia and high bit rate packet data.

Wideband CDMA has emerged as the mainstream air interface solution for the third generation networks. Wideband CDMA systems are currently being standardized by the European Telecommunications Standards Institute (ETSI) of Europe, the Association for Radio Industry and Business (ARIB) of Japan, the TIA Engineering Committees TR45 and TR46 and the T1 committee T1P1 of the United States, and the Telecommunication Technology Association TTA I and TTA II (renamed Global CDMA I and II, respectively) in Korea. The above description and a background of various systems can be found in WIDEBAND CDMA FOR THIRD GENERATION MOBILE COMMUNICATIONS by T. Ojanpera et al, published 1998, by Artech House Publishers, whose entire disclosure is hereby incorporated by reference therein.

Recently, ARIB in Japan, ETSI in Europe, T1 in U.S.A., and TTA in Korea have mapped out a third generation mobile communication system based on a core network and radio access technique of an existing global system for mobile communications (GSM) to provide various services including multimedia, such as audio, video and data. They have agreed to a partnership study for the presentation of a technical specification on the evolved next generation mobile communication system and named a project for the partnership study as a third generation partnership project (3GPP).

The 3GPP is classified into three part technical studies. The first part is a 3GPP system structure and service capability based on the 3GPP specification. The second part is a study of a universal terrestrial radio access network (UTRAN), which is a radio access network (RAN) applying wideband CDMA technique based on a frequency division duplex (FDD) mode, and a TD-CDMA technique based on a time division duplex (TDD) mode. The third part is a study of a core network evolved from a second generation GSM, which has third generation networking capabilities, such as mobility management and global roaming.

Among the technical studies of the 3GPP, the UTRAN study defines and specifies the transport and physical channels. This technical specification, TS S1.11 v1.1.0, was distributed on March of 1999, whose entire disclosure is hereby incorporated by reference therein. The physical channel includes the dedicated physical channels (DPCHs) used in the uplink and downlink. Each DPCH is generally provided with three layers, e.g., superframes, radio frames and timeslots. As specified in the 3GPP radio access network (RAN) standard, a superframe has a maximum frame unit of 720ms period. In view of the system frame numbers, one superframe is composed of seventy-two radio frames. Each radio frame has a period of 10ms, and a radio frame includes sixteen timeslots, each of which includes fields with corresponding information bits based on the DPCH.

Figure 4 illustrates a frame structure of an uplink DPCH based on the 3GPP RAN standard. The uplink DPCH is provided with two types of channels, e.g., a dedicated

physical data channel (DPDCH) and a dedicated physical control channel (DPCCH). The uplink DPDCH is adapted to transport the dedicated data and the uplink DPCCH is adapted to transport the control information.

The uplink DPCCH for the transport of the control information includes various fields such as a pilot field 21 of N_{pilot} bits, a transmit power-control (TPC) field 22 of N_{TPC} bits, a feedback information (FBI) field 23 of N_{FBI} bits and an optional transport-combination indicator (TFCI) field 24 of N_{TFCI} bits. The pilot field 21 includes pilot bits N_{pilot} for supporting channel estimation for coherent detection. The TFCI field 4 supports the simultaneous provision of a plurality of services by the system. The absence of the TFCI field 4 in the uplink DPCCH signifies that the associated service is a fixed rate service. The parameter k determines the number of bits per uplink DPDCH/DPCCH slot. It is related to the spreading factor SF of the physical channel as $SF=256/2^k$. The spreading factor SF may thus range from 256 down to 4.

Figure 5 is a table showing various information of the uplink DPCCH, wherein channel bit and symbol rates are those just prior to spreading. (At the time of this technical specification, the exact number of bits of the different uplink DPCCH fields of Figure 4 (N_{pilot}, N_{TPC}, N_{FBI}, and N_{TFCI}) was not determined.)

Figure 6 is a table illustrating pilot bit patterns of the uplink DPCCH, and more particularly, 6-bit and 8-bit pilot bit patterns for each slot. In Figure 6, the non-shaded sequence is used for channel estimation, and shaded sequence can be used as frame

synchronization words or sequences. The pilot bits other than frame synchronization word, e.g., channel estimation word, have a value of 1.

For example, in the case where each slot includes six pilot bits $N_{pilot} = 6$, the sequences formed by slot #1 to slot #16 at bit #1, at bit #2, at bit #4, and at bit #5 are used as the frame synchronization words. In the case where each slot is composed of eight pilot bits ($N_{pilot} = 8$), the sequences at bit #1, at bit #3, at bit #5, and at bit #7 are used as the frame synchronization words. In the case where the pilot bits of each sequences slot are either 6 or 8 in number, a total of four is used as the frame synchronization word. As a result, because one radio frame is provided with sixteen timeslots, the number of pilot bits used as the frame synchronization word is 64 bits per frame.

Figure 7 shows a spreading/scrambling arrangement for the uplink DPCH based on the 3GPP RAN standard. The arrangement of Figure 7 is provided for the execution of a quadrature phase shift keying (QPSK) operation where the uplink DPDCH and DPCCH are mapped into I and Q channel branches, respectively.

The spreading is an operation for switching all symbols through the respective channel branches to a plurality of chips. The I and Q channel branches are spread respectively at chip rates based on two different orthogonal variable spreading factors (OVSFs), or channelizing codes C_D and C_C. The OVSF represents the number of chips per symbol on each channel branch. The spread of two channel branches are summed and then complex-scrambled by a specific complex scrambling code C_{scramb}. The complex-

scrambled result is separated into real and imaginary and then transmitted after being placed on respective carriers.

Figure 8 illustrates a frame structure of a downlink DPCH based on the 3GPP RAN standard. The number of pilot bits (or symbols) in the uplink DPCH is 6 or 8 because the uplink DPCH is activated at a fixed rate of 16Kbps. However, since the downlink DPCH is activated at a variable rate, it has pilot symbol patterns illustrated in Figure 9.

With reference to Figure 8, similar to the uplink DPCH, the downlink DPCH is provided with two types of channels, e.g., a dedicated physical data channel (DPDCH) and a dedicated physical control channel (DPCCH). In the downlink DPCH, the downlink DPDCH is adapted to transport the dedicated data and the downlink DPCCH is adapted to transport the control information. The downlink DPCCH for transporting the control information is composed of various fields such as a pilot field 27, TPC field 26 and TFCI field 25. The pilot field 27 includes pilot symbols for supporting the channel estimation for coherent detection.

Figure 9 is a table illustrating pilot symbol patterns contained in the downlink DPCCH, which are classified according to different symbol rates of the downlink DPCCH. For example, in the case where the symbol rate is 16, 32, 64 or 128Kbps, each slot includes four pilot symbols for an I channel branch and four pilot symbols for a Q channel branch, totaling eight pilot symbols.

In Figure 9, the non-shaded sequence is used for channel estimation and shaded sequences can be used as frame synchronization words. The remaining pilot symbols other than the frame synchronization word (e.g., channel estimation) have a value of 11. For example, in the case where the symbol rate is 16, 32, 64 or 128Kbps, the sequences, formed by pilot symbols from slot #1 to slot #16, at symbol #1 and at symbol #3 are used as the frame synchronization words. Accordingly, because the number of pilot symbols used as the frame synchronization words is 4 per slot, 64 pilot symbols are used in each radio frame.

Figure 10 illustrates a spreading/scrambling arrangement for the downlink DPCH based on the 3GPP RAN standard. The arrangement of Figure 10 is provided for the spreading and scrambling of the downlink DPCH and a common control physical channel (CCPCH). A QPSK operation is performed with respect to a pair of symbols of the two channels in such a manner that they are serial-to-parallel converted and then mapped into I and Q channel branches, respectively.

The I and Q channel branches are spread respectively at chip rates based on two equal channelizing codes C_{ch}. The spread of the two channel branches are summed and then complex-scrambled by a specific complex scrambling code C_{scramb}. The complex-scrambled result is separated into real and imaginary and then transmitted, after being placed on respective carriers. Noticeably, the same scrambling code is used for all physical channels in one cell, whereas different channelizing codes are used for different physical

channels. Data and various control information are transported to a receiver through the uplink and downlink DPCHs subjected to the above-mentioned spreading and scrambling.

The TS S1.11 v1.1.0 specification also specified a primary common control physical channel (PCCPCH), which is a fixed rate downlink physical channel used to carry the broadcast channel (BCH), and a secondary common control physical channel (SCCPCH) used to carry the forward access channel (FACH) and the paging channel (PCH) at a constant rate. Figures 11A and 11B illustrate the frame structure of PCCPCH and SCCPCH, each having a pilot field. The TS S1.11 v1.1.0 specification recommended the pilot patterns for the PCCPCH and SCCPCH. Further, the TS S1.11 v1.1.0 specification recommended the pilot pattern of the DPCH channel for the diversity antenna using open loop antenna diversity based on space time block coding based transmit diversity (STTD) and diversity antenna pilot patterns for PCCPCH and SCCPCH. Those patterns can be found in the TS S1.11 v1.1.0 specification, and detailed description is being omitted.

For frame synchronization, an autocorrelation function must be performed on the basis of the pilot pattern sequence. In the pilot sequence design, finding an autocorrelation of a sequence with the lowest out-of-phase coefficient is important to decrease the probability of false alarm regarding the synchronization. A false alarm is determined when a peak is detected when there should not be a peak detection.

Optimally, the result of the autocorrelation for a frame with a sequence at a prescribed pilot bit should have same maximum values at zero and middle time shifts of one correlation period, which are different in polarity, and the remaining sidelobes at time shifts other than zero and middle should have a value of zero. However, the various pilot patterns recommended in the TS S1.11 v1.1.0 do not meet this requirement, both in the uplink and downlink.

In an article entitled "Synchronization Sequence Design with Double Thresholds for Digital Cellular Telephone" by Young Joon Song et al. (August 18-20, 1998), the present inventor being a co-author, the article describes a correlator circuit for GSM codes where the out-of-phase coefficients are all zero except one exception at zero and middle shift having a first peak and a second peak, where the first and second peaks are opposite in polarity, but the peaks are not equal to one another. Further, the article describes lowest out-of-phase coefficients of +4 and –4. However, the article does not provide how such sequences and autocorrelation can be used to achieve the above described optimal results, and the article does not provide sufficient disclosure that the sequences achieve or can achieve the lowest autocorrelation sidelobes.

As described above, the pilot patterns used as frame synchronization words or sequences do not achieve the optimal results. Further, the background pilot patterns do not rapidly and accurately perform the frame synchronization. Moreover, the above pilot patterns and frame synchronization sequences do not provide optimal cross-correlation

and autocorrelation. Additionally, neither the TS specification nor the article provides a solution of the use of the pilot patterns for slot-by-slot double check frame synchronization scheme, and neither discloses the use of the frame synchronization sequence for channel estimation.

SUMMARY OF THE INVENTION

An object of the present invention is to obviate at least the problems and disadvantages of the related art.

An object of the present invention is to provide frame synchronization words resulting in optimal autocorrelation results.

A further object of the present invention is to eliminate or prevent sidelobes.

A further object of the present invention is to provide maximum values at zero and middle time shifts.

Another object of the present invention is to provide a synchronization word for at least one of rapid and accurate frame synchronization.

Another object of the present invention is to provide a slot-by-slot double check frame synchronization scheme.

Still another object of the present invention is to provide a frame synchronization word which can be used for channel estimation.

Still another object of the present invention is to provide good cross-correlation and autocorrelation simultaneously.

An object of the invention is to provide a frame synchronization apparatus and method for accomplishing frame synchronization by using upward and downward link pilot patterns proposed in a 3GPP radio access network standard.

According to an aspect of the present invention, there is provided a frame synchronization method using an optimal pilot pattern including the steps of: storing column sequences demodulated and inputted by slots, in a frame unit, in detecting frame synchronization for upward and downward link channels; converting the stored column sequences according to a pattern characteristic related to each sequence by using the pattern characteristic obtained from the relation between the column sequences; adding the converted column sequences by slots; and performing a correlation process of the added result to a previously designated code column.

Preferably, the converting step comprises the steps of shifting, reversing and inverting the single column sequence to thereby generate the remaining column sequences.

According to another aspect of the present invention, there is provided a frame synchronization apparatus using an optimal pilot pattern including: a memory mapping/addressing block for converting column sequences inputted/demodulated by slots according to a defined pattern characteristic; an adder for adding the converted

outputs from the memory mapping/addressing block; and a correlator for performing a correlation process of the added result to a previously designated code column.

The present invention can be achieved in a whole or in parts by a method for synchronizing a frame using an optimal pilot symbol, comprising the steps of: (1) receiving a pilot symbol of each slot in the frame through respective physical channels on a communication link; (2) correlating a received position of each of the pilot symbols to a corresponding pilot sequence; (3) combining and summing more than one results of the correlations, and deriving a final result from the correlations in which sidelobes from the results of the correlations are offset; and (4) synchronizing the frame using the final result.

The pilot symbols are combined into each of the pilot sequences such that the final result of the correlations shows sidelobes with "0" values excluding particular positions of correlation periods. The particular positions are starting points (x = 0) of the correlation periods (x) and points of x /an integer. The pilot symbol is a combination of pilot symbols in a form of (a,/a). The pilot sequence provides least correlation resultants at positions excluding the starting points and half of the starting points in the correlation periods. The pilot symbols excluding the pilot symbols used in the correlation is used in a channel estimation for detecting coherent. The pilot symbol of each slot in the frame is transmitted, with the pilot symbol contained in a pilot field of an exclusive physical control channel among respective exclusive channels on the communication link. The pilot sequences different from each other on an up communication link are used in the

correlation according to values of bits included in a pilot field of an exclusive physical control channel. The pilot sequences different from each other on a down communication link are used in the correlation according to a symbol rate of an exclusive physical control channel.

The present invention can be also achieved in a whole or in parts by a method for synchronizing a frame using an optimal pilot symbol, comprising the steps of: (1) receiving a pilot symbol of each slot in the frame through respective physical channels on a communication link; (2) correlating a received position of each of the pilot symbols to a corresponding pilot sequence; (3) combining and summing more than one results of the correlations, and deriving a final result from the correlations in which sidelobes from the results of the correlations have minimum values and the results of the correlations at starting points and middle points of correlation periods have maximum values with different polarity; and (4) synchronizing the frame using the final result.

The present invention can be achieved in a whole or in parts by a method of eliminating sidelobes in a communication channel between a base station and a mobile station, comprising the steps of: generating control signals and data signals within the communication channel, the control signals having a first sequence of L-bits and a second sequence of L-bits; generating a first set of prescribed values based on the first sequence, which has a first prescribed relationship with the first set of prescribed values; generating a second set of prescribed values based on the second sequence, which has a second

prescribed relationship with the second set of prescribed values; and combining the first and second sets of prescribed values.

The present invention can be achieved in a whole or in parts by a method of establishing a communication channel, the method comprising the steps of: generating a plurality of frames; generating a L-number of slots for each frame, each slot having a pilot signal of N-bits and a corresponding bit in each slot forming a word of L-sequence of pilot bits such that there is N number of words, wherein the number of bit values of two pilot bits which are the same between two adjacent words from 1 to L slots minus the number of bit values of two pilot bits which are different between the two adjacent words from 1 to L is zero or a prescribed number close to zero.

The present invention can be achieved in a whole or in parts by a method of establishing a communication channel having at least one of frame synchronization and channel estimation, the method comprising the steps of: generating a plurality of frames; generating a L-number of slots for each frame, each slot having a pilot signal of N-bits and a corresponding bit in each slot forming a word of L-sequence of pilot bits such that there is N number of words, wherein the words have at least one of the following characteristics: cross-correlation between two adjacent sequences used for frame synchronization is zero at zero time shift, or cross-correlation between a word used for frame synchronization and a word used for channel estimation is zero at all time shifts.

The present invention can be achieved in a whole or in parts by a method of reducing sidelobes for frame synchronization, comprising the steps of: generating a plurality of frame synchronization words, each frame synchronization word having a plurality of bits; performing autocorrelation functions on a pair of frame synchronization words to generate a pair of prescribed value sets; and combining the pair of prescribed value sets such that two peak values equal in magnitude and opposite in polarity are achieved at zero and middle time shifts.

The present invention can be achieved in a whole or in parts by a method of generating pilot signals of a prescribed pattern within a frame having L-number of slots, comprising the steps of: generating N-number of pilot bits for each slot; and forming N-number of words of L-bit based on above step, wherein a prescribed number of words is used for frame synchronization words and each frame synchronization word has a first prescribed number b_0 of bit values of "0" and a second prescribed number b_1 of bit values of "1", such that b_1-b_0 is equal to zero or a number close to zero.

The present invention can be achieved in a whole or in parts by a communication link between a user equipment and a base station comprising a plurality of layers, wherein one of the layers is a physical layer for establishing communication between the user equipment and the base station and the physical layer has at least one of data and control information, one of the control information being a pilot field of N-bits transmitted for L-number of slots such that N-number of words of L-bit are formed, wherein cross-

correlation between two adjacent words used for frame synchronization is zero at zero time shift or cross-correlation between a word used for frame synchronization and a word used for channel estimation is zero at all time shifts.

The present invention can be achieved in a whole or in parts by a correlator circuit for at least one of a user equipment and a base station, comprising: a plurality of latch circuits, each latch circuit latching a word formed by a pilot bit from a plurality of slots; a plurality of correlators, each correlator coupled to a corresponding latch circuit and correlating the word to a set of prescribed values; and a combiner that combines the set from each correlator such that maximum peak values of equal in magnitude and opposite in polarity are formed at zero and middle time shifts.

The present invention can be achieved in a whole or in parts by a communication device comprising: means for transmitting at least one of data and control information; means for receiving at least one of data and control information, wherein the receiving means includes: a plurality of latch circuits, each latch circuit latching a word formed by a pilot bit from a plurality of slots; a plurality of correlators, each correlator coupled to a corresponding latch circuit and correlating the word to a set of prescribed values; a plurality of buffers, each buffer coupled to a corresponding correlator to store the set of prescribed values; and a combiner that combines the set from each buffer such that maximum peaks of equal in magnitude and opposite in polarity are formed at zero and middle time shifts.

Additional advantages, objects, and features of the invention will be set forth in part in the description which follows and in part will become apparent to those having ordinary skill in the art upon examination of the following or may be learned from practice of the invention. The objects and advantages of the invention may be realized and attained as particularly pointed out in the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention will be described in detail with reference to the following drawings in which like reference numerals refer to like elements wherein:

Figure 1 generally illustrates a system, which uses CDMA modulation techniques in communication between user and base stations;

Figure 2 illustrates these three different propagation phenomena;

Figure 3 depicts a block diagram of a transmitter and a receiver for time multiplexed pilot symbols;

Figure 4 illustrates a frame structure of an uplink DPCH based on the 3GPP RAN standard;

Figure 5 is a table showing various information of the uplink DPCCH;

Figure 6 is a table illustrating pilot bit patterns of the uplink DPCCH;

Figure 7 shows a spreading/scrambling arrangement for the uplink DPCH based on the 3GPP RAN standard;

Figure 8 illustrates a frame structure of a downlink DPCH based on the 3GPP RAN standard;

Figure 9 is a table illustrating pilot symbol patterns contained in the downlink DPCCH;

Figure 10 illustrates a spreading/scrambling arrangement for the downlink DPCH based on the 3GPP RAN standard;

Figures 11A and 11B illustrate the frame structure of PCCPCH and SCCPCH, respectively;

Figure 12A is a table illustrating the frame synchronization words C_1 to $C_{i\text{-}th}$ in accordance with a preferred embodiment of the present invention;

Figure 12B is a table illustrating the autocorrelation function of the sequences of pilot bits;

Figure 13A illustrates addition of two autocorrelation functions;

Figure 13B illustrates addition of the four autocorrelation functions;

Figures 14A and 14B are tables illustrating the pilot patterns in accordance with a preferred embodiment of the present invention for uplink DPCCH;

Figure 14C is a table illustrating the mapping relationship between the 8 synchronization words C_1-C_8 of Figure 12A and shaded pilot bit patterns of Figures 14A and 14B;

Figure 14D illustrates a correlation circuit for frame synchronization based on pilot bits of the uplink DPCCH in accordance with a preferred embodiment of the present invention;

Figure 14E is a table illustrating the correlation results at points A_1-A_4, and the summing of the correlation results at point B of Figure 14D.

Figure 14F is a table illustrating various results of the addition of correlation results based on the uplink pilot patterns of the frame synchronization words in accordance with the preferred embodiment of the present invention;

Figure 14G illustrates a correlator circuit for frame synchronization based on pilot bit sequences of an uplink DPCCH in accordance with an alternative embodiment;

Figure 14H illustrates the receiver circuit of a base station or a user equipment to recover the received spread signal including the frame synchronization words in the pilot field;

Figure 14I illustrates results of correlation circuit using the pilot pattern of the technical specification;

Figure 14J illustrates a time shift graph of the summation of results of Figure 14I;

Figure 15A illustrates the pilot symbol patterns for downlink DPCH;

Figure 15B illustrates the mapping relationship between the 8 frame synchronization words of Figure 12A, and shaded pilot symbol pattern of Figure 15A;

Figure 15C illustrates a correlation circuit for frame synchronization for downlink DPCCH in accordance with the preferred embodiment;

Figure 16A illustrates pilot symbol pattern of PCCPCH;

Figure 16B illustrates the mapping relationship between the synchronization words C_1-C_8 of Figure 12A, and the shaded pilot symbol patterns of Figure 16A;

Figure 16C illustrates pilot symbol pattern of SCCHPCH;

Figure 16D illustrates the mapping relationship between the synchronization words C_1-C_8 of Figure 12A, and the shaded pilot symbol patterns of Figure 16C;

Figures 17A-17C illustrate addition of autocorrelation functions of frame synchronization word of the preferred embodiment and current pilot patterns (described in TS S1.11 v1.1.0 specification) for DPCHs and PCCPCH;

Figure 18A illustrates the parameters used for obtaining P_D, P_{FA}, and P_S on uplink DPCCH and downlink DPCH over additive white Gaussian noise (AWGN);

Figure 18B illustrates the probability of detection P_D on downlink DPCCH over AWGN channel;

Figure 18C illustrates the probability of false alarm P_{FA} on downlink DPCCH over AWGN channel;

Figure 18D illustrates the probability of a frame synchronization confirmation success P_S on downlink DPCCH over AWGN channel;

Figure 19A illustrates pilot symbol patterns of downlink DPCH for the diversity antenna using a space time block coding based transmit diversity (STTD);

Figure 19B illustrates the mapping relationship between the 8 words C_1-C_8 of Figure 12A and shaded pilot symbol patterns of Figure 19A;

Figure 19C illustrates the diversity antenna pilot symbol pattern for PCCPCH;

Figure 19D illustrates the mapping relationship between the words C_1-C_8 of Figure 12A and shadowed pilot symbol patterns of Figure 19C;

Figure 19E illustrates the pilot symbol pattern for the diversity antenna when STTD encoding is used on the SCCPCH;

Figure 19F illustrates the mapping relationship between the words C_1-C_8 of Figure 12A and shaded pilot symbol patterns of Figure 19E;

Figure 20A is a table illustrating frame synchronization words C_1-C_{16} (i=16) and autocorrelated function in accordance with another preferred embodiment of the present invention;

Figure 20B is a table illustrating the autocorrelation function of the pilot bits of each frame synchronization word classified in the PCSP;

Figure 20C illustrates the pilot bit pattern of uplink DPCCH;

Figure 20D illustrates a mapping relationship between the alternative frame synchronization words C_1-C_{16} of Figure 20A and the shaded frame synchronization words of Figure 20C;

Figures 20E and 20F illustrate the pilot symbol pattern of downlink DPCH;

Figure 20G illustrates a mapping relationship between the alternative frame synchronization words C_1-C_{16} of Figure 20A and the shaded frame synchronization words of Figures 20E and 20F;

Figure 20H illustrates the pilot symbol pattern of downlink PCCPCH;

Figure 20I illustrates a mapping relationship between the alternative frame synchronization words C_1-C_{16} of Figure 20A and the shaded frame synchronization words of Figure 20H.

Figure 21 illustrates a preferred embodiment for the new frame synchronization words C_1-$C_{i\text{-}th}$;

Figure 22A illustrates the addition of two auto-correlation functions;

Figure 22B illustrates the addition of two cross-correlation functions between the two frame synchronization words within the same class;

Figure 22C illustrates the addition of four auto-correlation functions;

Figure 22D illustrates the addition of four cross-correlation functions between the four frame synchronization words of two classes;

Figures 23A illustrates the pilot bit patterns on uplink DPCCH with N_{pilot} = 2, 3, and 4;

Figure 23C illustrates the pilot bit patterns on uplink DPCCH with N_{pilot} = 2,3, and 4 in accordance with an alternative embodiment compared to Figure 23A;

Figures 23E and 23F illustrate the pilot bit patterns on uplink DPCCH with N_{pilot} = 5, 6, 7, and 8;

Figures 23B and 23D illustrate the mapping relationship between the frame synchronization words of Figure 21, and shaded frame synchronization words of Figures 23A and 23D, respectively;

Figure 23G illustrates the mapping relationship between the frame synchronization words of Figure 21, and the shaded frame synchronization words of Figures 23E and 23F;

Figure 23H illustrates the structure of random access channel;

Figure 23I illustrates the random access message control fields;

Figure 23J illustrates the pilot bit pattern of the RACH;

Figure 24A illustrates the pilot symbol patterns on downlink DPCH when N_{pilot} = 2, 4, 8, and 16;

Figure 24B illustrates the mapping relationship between the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 24A;

Figure 24C illustrates the pilot symbol patterns of downlink DPCH for the diversity antenna using STTD;

Figure 24D illustrates the mapping relationship between the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 24C;

Figure 25A illustrates the pilot symbol patterns for downlink SCCPCH for N_{pilot} = 8 and 16;

Figure 25B illustrates the mapping relationship of the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 25A;

Figure 25C illustrates the pilot symbol patterns of downlink SCCPCH for Npilot = 8 and 16 for the diversity antenna using STTD;

Figure 25D illustrates the mapping relationship between the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 25C;

Figure 26A illustrates the parameters used to evaluate the performance of the pilot bit pattern on uplink DPCCH over AWGN;

Figure 26B illustrates the probability of frame synchronization confirmation success P_S on uplink DPCCH with N_{pilot} =6 over AWGN channel;

Figure 26C illustrates the probability of a false alarm P_{FA} on uplink DPCCH with N_{pilot} =6 over AWGN channel;

Figure 27 is a comparison chart between the embodiments for 15 timeslots and 16 slots;

Figure 28A is a block diagram of an STTD transmitter according to the 3GPP RAN standards;

Figure 28B illustrates an STTD encoding based on the STTD transmitter of Figure 28A;

Figures 29A and 29B are graphs illustrating an embodiment of correlation results using a pilot pattern in accordance with a preferred embodiment of the present invention;

Figures 30A and 30B are graphs illustrating another embodiment of correlation results using a pilot pattern in accordance with a preferred embodiment of the present invention;

Figure 31 illustrates a correlation processing apparatus for an uplink channel in accordance with a preferred embodiment of the present invention;

Figure 32 illustrates a correlation processing apparatus for a downlink channel in accordance with a preferred embodiment of the present invention; and

Figure 33 is a graph illustrating the correlation result of the correlation processing apparatus of Figure 32.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

The new frame synchronization words in accordance with the preferred embodiment have the lowest out-of-phase values of autocorrelation function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts. The frame synchronization words are suitable for frame synchronization confirmation since by simply adding autocorrelation functions of such words, double maximum correlation values equal in magnitude and opposite polarity at zero and middle shifts can be achieved. This property can be used to double-check frame synchronization timing and reduce the synchronization search time.

The UE establishes downlink chip synchronization and frame synchronization based on the Primary CCPCH synchronization timing and the frame offset group, slot offset group notified from the network. The frame synchronization can be confirmed using the frame synchronization word. The network establishes uplink channel chip synchronization and frame synchronization based on the frame offset group and slot offset group. The frame synchronization can also be confirmed using the frame synchronization word.

When long scrambling code is used on uplink channels or downlink channels, failure in frame synchronization confirmation using frame synchronization words always means losing frame and chip synchronizations since the phase of long scrambling code repeats every frame. Whereas in the case of short scrambling code on uplink DPCCH, failure in frame synchronization confirmation does not always implies losing chip synchronization since the length of short scrambling code is 256 and it corresponds to one symbol period of uplink DPCCH with SF = 256. Thus, the frame synchronization word of pilot pattern can detect synchronization status and this information can be used in RRC Connection Establishment and Release Procedures of Layer 2.

Figure 12A is a table illustrating the frame synchronization words C_1 to $C_{i\text{-}th}$ in accordance with a preferred embodiment of the present invention, where each word comprises L number ($L > 1$) of sequence of pilot bits from a prescribed bit position of the N_{pilot} bits ($N_{pilot} > 0$) from each slot of L number of slots. In the preferred first

embodiment described hereinafter, the number of synchronization words i equals 8, the number of slots L = 16 and the number of pilot bits N_{pilot} in each slot is between 4 and 16, but the present invention is applicable to different variations of i, L, and N_{pilot}.

The synchronization words C_1-C_8 of the preferred embodiment can be divided into 4 classes (E-H, referred to as Preferred Correlation Sequence Pair (PCSP)) according to the autocorrelation function of the synchronization words, as follows:

$$E = \{C_1, C_5\}$$
$$F = \{C_2, C_6\}$$
$$G = \{C_3, C_7\}$$
$$H = \{C_4, C_8\}$$

Figure 12B is a table illustrating the autocorrelation function of 1 to 16 sequences of pilot bits of each frame synchronization word classified in classes E, F, G and H within one correlation period from a time shift of 0 to 15. As shown in Figures 12A and 12B, each class contains 2 sequences, and sequences of the same class have the same autocorrelation function. From Figure 12B, the synchronization words have the lowest out-of-phase values of autocorrelation function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts. Moreover, the results R_1 and R_2 of the autocorrelation function are complements of each other. The following relationships between the autocorrelation functions are expressed in equations (1)-(4):

$$R_E(\tau) = R_F(\tau) = R_G(\tau) = R_H(\tau), \ \tau \text{ is even} \quad (1)$$

$$R_E(\tau) = -R_F(\tau)\ ,\ \tau \text{ is odd} \quad (2)$$

$$R_G(\tau) = -R_H(\tau)\ ,\ \tau \text{ is odd} \quad (3)$$

$$R_i(\tau) + R_i(\tau + 8) = 0\ ,\ i \in \{E,F,G,H\}, \text{ for all } \tau \quad (4)$$

From equations (1), (2), and (3), the following equation is obtained.

$$R_E(\tau) + R_F(\tau) = R_G(\tau) + R_H(\tau)\ , \text{ for all } \tau \quad (5)$$

The addition of two autocorrelation functions $R_E(\tau)$ and $R_F(\tau)$, or $R_G(\tau)$ and $R_H(\tau)$ becomes the function with two peak values equal in magnitude and opposite in polarity at zero and middle shifts, and all zero values except the zero and middle shifts, which is depicted in Figure 13A, where the peak values equal 2*L or –2*L. In the preferred embodiment, the peak values of Figure 13A are 32 and -32, since L=16. The other combinations such as $(R_E(\tau) + R_G(\tau))$, $(R_E(\tau) + R_H(\tau))$, $(R_F(\tau) + R_G(\tau))$, and $(R_F(\tau) + R_H(\tau))$ do not have the same value as in Figure 13A. By using the derived properties of the frame synchronization words, the following property is achieved.

$$\sum_{i=1}^{2\alpha} R_i(\tau) = \alpha \cdot (R_E(\tau) + R_F(\tau)), 1 \le \alpha \le 4 \quad (6)$$

where $R_i(\tau)$ is the autocorrelation function of sequence C_i, $1 \le i \le 8$.

The addition of the four autocorrelation functions is illustrated in Figure 13B, which is the same as Figure 13B except that the maximum value is doubled to 4*L or –4*L (the maximum values being 64 and -64 for the preferred embodiment) since $(R_E(\tau) + R_F(\tau) + R_G(\tau) + R_H(\tau)) = 2\ (R_E(\tau) + R_F(\tau))$ by equations (5) and (6). This property allows the

double-checking of the frame synchronization timing and the reduction of the synchronization search time.

First Embodiment for Uplink DPCCH

Figures 14A and 14B are tables illustrating the pilot patterns in accordance with a preferred embodiment of the present invention for uplink DPCCH with N_{pilot} = 5, 6, 7, and 8. The shaded pattern of Figures 14A and 14B are used for frame synchronization (which can also be used for channel estimation), and the pilot bit other than the frame synchronization words (e.g., channel estimation) has a value of 1. Figure 14C is a table illustrating the mapping relationship between the 8 synchronization words C_1-C_8 of Figure 12A and shaded pilot bit patterns of Figures 14A and 14B, where frame synchronization words C_1, C_2, C_3, and C_4 are the elements of the set {E, F, G, and H}, respectively. The results of Figures 13A and 13B are obtained by α = 1 and 2 in equation (6), respectively, which allows a double-check of the frame synchronization timing and a reduction of the synchronization time on uplink DPCCH with N_{pilot} = 5, 6, 7, and 8.

For example, the frame synchronization words at bit #1 (C_1), at bit #2 (C_2), at bit #4 (C_3) and at bit #5 (C_4) are used in the autocorrelation process for the frame synchronization when N_{pilot}=6. For N_{pilot}=8, the frame synchronization words at bit #1 (C_1), at bit #3 (C_2), at bit #5 (C_3) and at bit #7 (C_4) are used in the autocorrelation process for the frame synchronization. For N_{pilot}=5, 6, 7, and 8 in each slot, a total of four frame

synchronization words are used. As a result, since one radio frame has sixteen timeslots, the number of pilot bits used for the frame synchronization is only 64 per frame in the preferred embodiment. As can be appreciated, the number of words used for frame synchronization can vary depending on variations of N_{pilot}. For example, when $N_{pilot}=1$, one of the frame synchronization words C_1-C_8 can be used for both frame synchronization and channel estimation due to the novel feature of the preferred embodiment.

With the implementation of the novel pilot patterns, the values for the number of bits per field are shown below in Table 1and Table 2, with reference to Figure 4. The channel bit and symbol rates given in Table 1 are the rates immediately before spreading.

Table 1: DPDCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
16	16	256	160	10	10
32	32	128	320	20	20
64	64	64	640	40	40
128	128	32	1280	80	80
256	256	16	2560	160	160
512	512	8	5120	320	320
1024	1024	4	10240	640	640

There are two types of Uplink Dedicated Physical Channels; those that include TFCI(e.g. for several simultaneous services) and those that do not include TFCI(e.g.

for fixed-rate services). These types are reflected by the duplicated rows of Table 2. The channel bit and symbol rates given in Table 2 are the rates immediately before spreading.

Table 2: DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}
16	16	256	160	10	6	2	2	0
16	16	256	160	10	8	2	0	0
16	16	256	160	10	5	2	2	1
16	16	256	160	10	7	2	0	1
16	16	256	160	10	6	2	0	2
16	16	256	160	10	5	1	2	2

Figure 14D illustrates a correlation circuit for frame synchronization based on pilot bits of the uplink DPCCH in accordance with a preferred embodiment of the present invention when frame synchronization words C_1-C_4 are used. The frame synchronization words C_1-C_4 are latched in latch circuits 31-34, respectively. The correlators 41-44 perform correlation function R(x), where x=0 to L-1,of the frame synchronization words C_1-C_4, respectively, to generate the correlation results A_1-A_4, which are stored in buffers 51-53.

Figure 14E is a table illustrating the correlation results at points A_1-A_4, and the summing of the correlation results at point B. As shown, the result has maximum values of opposite polarity at zero and middle time shifts R(0) and R(8). Further, the remaining sidelobes at time shifts other than zero and middle have values of zero after the addition

at point B. The sidelobes are eliminated or minimized, and the results at point B correspond to the optimal results of Figure 13B.

Figure 14F is a table illustrating various results of the addition of correlation results of points A_1-A_4 based on the uplink pilot patterns of the frame synchronization words C_1-C_4 in accordance with the preferred embodiment of the present invention. The respective addition of the autocorrelation results of points (A_1+A_2), (A_3+A_4), (A_1+A_4) and (A_2+A_3) exhibit the same characteristics of the optimal results illustrated in Figure 13A.

Figure 14G illustrates a correlator circuit for frame synchronization based on pilot bit sequences of an uplink DPCCH in accordance with an alternative embodiment. The elements are the same as the correlator circuit of Figure 14D. The frame synchronization words of (C_1 and C_2), (C_2 and C_3), (C_3 and C_4), or (C_4 and C_1) are correlated and summed to provide the results at point D. The summation result at point D of Figure 14G is similar to the correlator circuit of Figure 14D other than the maximum values of opposite polarity being 2*L (32) and -2*L (-32), rather than 4*L (64) and -4*L (-64), respectively, corresponding to the results of Figure 14F and optimal results of Figure 13A.

Figure 14H illustrates the receiver circuit 60 of a base station or a user equipment to recover the received spread signal including the frame synchronization words in the pilot field. After despreading the received spread signal by the despreading circuit 61, the channel estimator and frame synchronizer 62 performs the channel estimation and the frame synchronization based on the pilot field. The Rake combiner 63 uses the results

of the channel estimator and frame synchronizer, and after rake combining, the data is deinterleaved by the deinterleaving circuit 64 in the reverse order of the transmitter side. Thereafter, the data is recovered after decoding by a decoder 65.

The advantages of the present invention can be readily discerned based on comparison of the frame synchronization words previously recommended in TS S1.11 v1.1.0 specification and the frame synchronization words for, e.g., $N_{pilot}=6$. Applying the same principle of equations (1)-(6) and the correlator circuit of Figure 14D, the results in Figure 14I are obtained for the pilot pattern indicated in the technical specification. When the summation result at point B is mapped on a time shift graph, the problem of sidelobes is readily apparent, as shown in Figure 14J. In other words, there is no maximum peak values of opposite polarity at zero and middle time shifts, and sidelobes are present at time shifts other than zero and middle.

As described in the background art, obtaining good cross-correlation and autocorrelation simultaneous is difficult to achieve, where cross-correlation relates to different words at different time shifts and autocorrelation relates to same sequences which are time shifted version. The good cross-correlation and autocorrelation of the present invention is based on unique properties of the frame synchronization words.

The unique characteristics of the frame synchronization words in accordance with the preferred embodiment can be readily discerned in view of Figures 12, 14A and 14B. As shown in frame synchronization words C_1-C_8 of Figure 12, each word has substantially

the same number of 1 and 0. In other words, the number (b_1) of pilot bits of a frame synchronization words having a value of 1 minus the number (b_0) of pilot bits of the frame synchronization having a value of 0 is equal to zero or close to zero. In the preferred embodiment, when there are even number of slot numbers, there are the same number of pilot bits having a value of 1 and 0 in a single frame synchronization word such that b_1-b_0 is zero. As can be appreciated, when there are an odd number of pilot bits in a single frame synchronization word, the result of b_1-b_0 is plus or minus one, e.g., close to zero.

The second characteristic of the frame synchronization words can be discerned by an examination between a pair of adjacent frame synchronization words (shaded patterns of Figures 14A and 14B for N_{pilot}=5, 6, and 7), or between a pair of adjacent frame synchronization word and channel estimation word (shaded and non-shaded patterns of Figures 14A and 14B for N_{pilot}=5, 6, 7, and 8). Generally, the number (b_3) of bit values which are the same (0, 0 and 1,1) between a pair of adjacent words (i.e., between two adjacent frame synchronization words, or between a frame synchronization word and a channel estimation word, which are adjacent) minus the number (b_4) of bit values which are different (1,0 or 0,1) between adjacent words (i.e., between two adjacent frame synchronization words, or between a frame synchronization word and a channel estimation word, which are adjacent) equals zero or a prescribed number close to zero.

In the preferred embodiment, the number (b_3) of pilot bit values which are the same between two adjacent words equals the number (b_4) of pilot bit value which are different between the two adjacent words, i.e., b_3-b_4=0. In the preferred embodiment, when the N_{pilot}=5, between two synchronization words of C_1 at bit #0 and C_2 at bit #1, there same number of pilot bit values which are the same (0,0 and 1,1) and pilot bit values which are different (1,0 and 0,1) from slot #1 to slot #16, as shown in Figure 14A. Similarly, between a synchronization word C_2 at bit #1 and a channel estimation word at bit #2, there same number of pilot bit values which are the same (0,0 and 1,1) and pilot bit values which are different (1,0 and 0,1) from slot #1 to slot #16. The same applies between two adjacent words at bit #2 and bit #3, and between two adjacent words at bit #3 and bit #4. The above also applies to adjacent words of N_{pilot}=6, 7 and 8. As can be appreciated, when an odd number of slots are used, the result of b_3-b_4 equals plus or minus one, e.g., close to zero.

As a result of such a characteristic, cross-correlation between two adjacent words used for frame synchronization is zero (orthogonal) at zero time shift. Further, the cross-correlation between a word used for frame synchronization and the sequence used for channel estimation is zero (orthogonal) at all time shifts. In other word, within N_{pilot} number of words of L-bits, there are an even number of words used for frame synchronization, but all words perform channel estimation, wherein between adjacent words used for frame synchronization, there is substantially zero cross-correlation.

Moreover, the words used for frame synchronization has substantially zero cross-correlation with words not used for frame synchronization, i.e., channel estimation, at any time shifts.

Further, each N_{pilot} words corresponds to a prescribed number by an autocorrelation function such that when a pair from a set of autocorrelated results corresponding to words used for frame synchronization is combined, two peak values equal in magnitude and opposite in polarity are achieved at zero and middle time shift while sidelobes are substantially eliminated at time shifts other than zero and middle. Autocorrelation in accordance with the present invention can be generally defined as a correlation between a word and its time shifted replica (including replica at zero time shift), where correlation is the number of bit values which are the same between two words minus the number of bit values which are different between the same two words. Further, as shown in Figure 12B, R_1 and R_2 are complements of each other.

First Embodiment for Downlink DPCH

Figure 15A illustrates the pilot symbol patterns for downlink DPCH for $N_{pilot}=4$, 8 and 16, where two pilot bits form a symbol since the left bit is used for the I channel branch and the right bit is used for the Q channel branch. In the preferred embodiment, $N_{pilot}=4$ can be used for 8 ksps (kilo symbols per second); $N_{pilot}=8$ can be used for 16, 32,

64, and 128 ksps; and $N_{pilot}=16$ can be used for 256, 512, and 1024ksps. The shaded symbols of Figure 15A can be used for frame synchronization, and the value of pilot symbol other than for frame synchronization word, e.g., channel estimation (channel estimation word), is 11. The results of Figure 15A is obtained by allowing $\alpha = 1$ for $N_{pilot}=4$, $\alpha = 2$ for $N_{pilot}=8$, and $\alpha = 4$ for $N_{pilot}=16$ in equation (6) for downlink DPCH.

Figure 15B illustrates the mapping relationship between the 8 frame synchronization words of Figure 12A, and shaded pilot symbol pattern of Figure 15A. For example, in the preferred embodiment of $N_{pilot}=4$, the symbol #1 includes two frame synchronization words of C_1 (for the I channel branch I-CH, i.e., left sequence of bits from slot #1 to slot #16) and C_2 (for the Q channel branch Q-CH, i.e., right sequence of bits from slot #1 to slot #16). For $N_{pilot}=8$ and $N_{pilot}=16$, the correspondence of words to channels for corresponding symbols is self-explanatory in Figure 15B. Similar to the uplink DPCCH, slot-by-slot double-check of the frame synchronization timing and a reduction of the frame synchronization search time can be achieved by using the autocorrelation property of the pilot symbol pattern based on equation (6).

Because the frame synchronization words of the downlink DPCH is based on frame synchronization words of Figure 12A, the characteristics described for uplink DPCCH is applicable to downlink DPCH. For example, the number (b_3) of bit values which are the same (0,0 and 1,1) between adjacent words (i.e., between synchronization word of I channel branch and synchronization word of Q channel branch of a frame

synchronization symbol, or between a channel estimation word of the Q channel branch and a frame synchronization word of the I channel branch, which are adjacent, or between a frame synchronization word of the Q channel branch and a channel estimation word of the I channel branch, which are adjacent) minus the number (b_4) of bit values which are different (1,0 and 0,1) between adjacent words (i.e., between synchronization word of I channel branch and synchronization word of Q channel branch of a frame synchronization symbol, or between a channel estimation word of the Q channel branch and a frame synchronization word of the I channel branch, which are adjacent, or between a frame synchronization word of the Q channel branch and a channel estimation word of the I channel branch, which are adjacent) equals zero or a prescribed number close to zero.

For example, for $N_{pilot}=8$, between the symbols #0 and #1, the number of a pair of adjacent bits, i.e., one bit from the Q channel branch of the symbol #0 and one bit from the I channel branch of the symbol #1, having bit values of 1,1 and 0,0 is the same as the number of adjacent bits having bit values of 1,0 and 0,1. In other words, b_3-$b_4=0$. As can be appreciated, if the number of slots L is an odd number, the result of b_3-b_4 is plus or minus one, e.g., a prescribed number close to zero.

With the implementation of the novel pilot symbols, the below Table 3 shows the number of bits per slot of the various fields with reference to Figure 8. There are basically two types of downlink Dedicated Physical Channel; those that include TFCI (e.g. for

several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of Table 3. The channel bit and symbol rates given in Table 3 are the rates immediately before spreading. If there is no TFCI, then the TFCI field is left blank (*).

Table 3: DPDCH and DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
			DPDCH	DPCCH	TOT		N_{Data1}	N_{Data2}	N_{TFCI}	N_{TPC}	N_{Pilot}
16	8	512	64	96	160	10	2	2	0	2	4
16	8	512	32	128	160	10	0	2	2	2	4
32	16	256	160	160	320	20	2	8	0	2	8
32	16	256	128	192	320	20	0	8	2	2	8
64	32	128	480	160	640	40	6	24	0	2	8
64	32	128	448	192	640	40	4	24	2	2	8
128	64	64	960	320	1280	80	4	56	8*	4	8
256	128	32	2240	320	2560	160	20	120	8*	4	8
512	256	16	4608	512	5120	320	48	240	8*	8	16
1024	512	8	9728	512	10240	640	112	496	8*	8	16
2048	1024	4	19968	512	20480	1280	240	1008	8*	8	16

Figure 15C illustrates a correlation circuit for frame synchronization for downlink DPCCH of $N_{pilot}=8$ in accordance with the preferred embodiment. The operation and components are the same as the correlation circuit of Figure 14D for uplink DPCCH, except for the reception of I channel branch and Q channel branch synchronization

words. The results of points A_1-A_4 and point B is the same as Figure 14E. Similarly, the sidelobes are eliminated or minimized, and the results correspond to the optimal results of Figure 13B. Because the number of pilot symbols (or pilot bits) used for the frame synchronization is 2 symbols per slot (or 4 bit per slot), 32 pilot symbols (or 64 pilot bits) are used in each radio frame for the frame synchronization.

For $N_{pilot}=4$ in the downlink DPCCH, the correlator circuit of Figure 14G can be used. In such a case, the I and Q channel frame synchronization words are inputted to the correlator circuit. The summation result would be the same as Figure 14F, which corresponds to the optimal results of Figure 13A. In this case, the number of pilot symbols (or pilot bits) used for the frame synchronization is 1 symbol per slot (or 2 bits per slot), and 16 symbols (or 32 pilot bits) are used in each radio frame for the frame synchronization.

As per $N_{pilot}=16$ in the downlink DPCCH, the correlation circuit of Figure 15C can be expanded to accommodate the additional frame synchronization words of the I and Q channel branches of pilot symbol #5 and symbol #7. The summation result would be similar to the optimal results of Figure 13B, but the maximum peak values of opposite polarity would be 128 (8*L) and -128 (-8*L). Further, the number of pilot symbols (or pilot bits) used for the frame synchronization is 4 symbols per slot (or 8 bits per slot), and 64 pilot symbols (or 128 pilot bits) are used in each radio frame for the frame synchronization.

First Embodiment of Downlink PCCPCH and SCCPCH

Figure 16A illustrates pilot symbol pattern of PCCPCH. The shaded symbols can be used for frame synchronization, and the value of pilot symbol other than for frame synchronization is 11. Figure 16B illustrates the mapping relationship between the synchronization words C_1-C_8 of Figure 12A, and the shaded pilot symbol patterns of Figure 16A. A double-check frame of the synchronization timing and the reduction of the synchronization search time can be achieved with $\alpha = 1$ or 2 in equation (6).

Figure 16C illustrates pilot symbol pattern of SCCPCH. The shaded symbols can be used for frame synchronization, and the value of pilot symbol other than for frame synchronization is 11. Figure 16D illustrates the mapping relationship between the synchronization words C_1-C_8 of Figure 12A, and the shaded pilot symbol patterns of Figure 16C.

As shown above, the frame synchronization words of PCCPCH and SCCPCH is based on the frame synchronization words C_1-C_8, and the disclosure for the uplink DPCCH and the downlink DPCH is applicable. Hence, a detailed description regarding the various characteristics including cross-correlation and autocorrelation, operations and implements are omitted since one of ordinary skill in the art can readily appreciate the present invention based on the uplink DPCCH and downlink DPCH.

As described above, the non-shaded symbols are the pilot symbols not used for frame synchronization comprises symbols of 11, and the shaded symbols are used for frame synchronization. The frame synchronization words of the pilot pattern are used for frame synchronization confirmation, and the summation of autocorrelated values for each frame synchronization words is required. The property of summation of autocorrelated values of frame synchronization words is very important.

With the implementation of the novel pilot symbols, the values for the number of bits per field are given in Table 4 with reference to Figure 11B. The channel bit and symbol rates given in Table 4 are the rates immediately before spreading.

Table 4: Secondary CCPCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
32	16	256	320	20	12	8	0
32	16	256	320	20	10	8	2
64	32	128	640	40	32	8	0
64	32	128	640	40	30	8	2
128	64	64	1280	80	72	8	0
128	64	64	1280	80	64	8	8
256	128	32	2560	160	152	8	0
256	128	32	2560	160	144	8	8
512	256	16	5120	320	304	16	0
512	256	16	5120	320	296	16	8
1024	512	8	10240	640	624	16	0
1024	512	8	10240	640	616	16	8
2048	1024	4	20480	1280	1264	16	0
2048	1024	4	20480	1280	1256	16	8

The addition of autocorrelation functions of frame synchronization word of the preferred embodiment and current pilot patterns (described in TS S1.11 v1.1.0 specification) for DPCHs and PCCPCH are depicted in Figures 17A (N_{pilot} =4), Figure 17B (N_{pilot} =8) and Figure 17C (N_{pilot}=16). As shown, the current pilot patterns have non-zero out-of-phase autocorrelation function with peak value at zero shift, whereas the frame synchronization words of the preferred embodiment have zero out-of-phase autocorrelation function with two peak values equal in magnitude and opposite in polarity at zero and middle time shifts (delays).

Correlation to a prescribed frame synchronization word is optimum method for frame synchronization. Since the frame synchronization word of pilot pattern is used for frame synchronization confirmation, the following events and parameters are used to evaluate the performance of frame synchronization confirmation using the frame synchronization words of the preferred embodiment and the current pilot patterns:

H_1 : The event that the correlator output exceeds the predetermined threshold when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is zero.

H_2 : The event that the correlator output exceeds the predetermined threshold when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is not zero.

H_3 : One event of H_1 and no event of H_2 for one frame.

H_4 : The event that the correlator output exceeds the predetermined threshold or is smaller than −1×(predetermined threshold) when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is 0 or 8, respectively.

H_5 : The event that the correlator output exceeds the predetermined threshold or is smaller than −1×(predetermined threshold) when the code phase offset between the received shadowed column frame synchronization word and its corresponding receiver stored frame synchronization word is not 0 and 8.

H_6 : One event of H_4 and no event of H_5 for one frame.

P_D : Probability of a detection.

P_{FA} : Probability of a false alarm.

P_S : Probability of a frame synchronization confirmation success for one frame.

From the above definitions, when the current pilot pattern is used for frame synchronization confirmation, the probability of a detection and a false alarm can be expressed as:

$$P_D = \text{Prob}(H_1) \tag{7}$$

$$P_{FA} = \text{Prob}(H_2) \tag{8}$$

The probability of a frame synchronization confirmation success for one frame becomes $P_S = \text{Prob}(H_3)$ and it can be expressed as

$$P_S = P_D(1-P_{FA})^{15} \quad (9)$$

Whereas in the case of the frame synchronization words of the preferred embodiment, as has been stated, double thresholds are needed for double-check frame synchronization, and the probability of a detection and a false alarm can be expressed as:

$$P_D = \text{Prob}(H_4) \quad (10)$$

$$P_{FA} = \text{Prob}(H_5) \quad (11)$$

Similarly, in the case of frame synchronization words of the preferred embodiment, the probability of a frame confirmation success for one frame becomes $P_S = \text{Prob}(H_6)$ and it is given by

$$P_S = P_D(1-P_{FA})^{14} \quad (12)$$

From equations (9) and (12), the probability of a frame synchronization confirmation is greatly affected by the probability of a false alarm since P_S is proportional to P_D and $(1-P_{FA})^{14}$ or $(1-P_{FA})^{15}$. For example, assume that $P_{FA} = 10^{-1}$, then $(1-P_{FA})^{14} = 0.2288$ and $(1-P_{FA})^{15} = 0.2059$. Now let $P_{FA} = 10^{-3}$, then $(1-P_{FA})^{14} = 0.9861$ and $(1-P_{FA})^{15} = 0.9851$. The performance of frame synchronization can be sufficiently evaluated by selecting the threshold so that the P_{FA} is much smaller than $(1-P_D)$.

The parameters of Figure 18A are used for obtaining P_D, P_{FA}, and P_S on uplink DPCCH and downlink DPCH over additive white Gaussian noise (AWGN). Figure 18B

illustrates the probability of detection P_D on downlink DPCCH with $N_{pilot}=4$ over AWGN channel, Figure 18C illustrates the probability of false alarm P_{FA} on downlink DPCCH with $N_{pilot}=4$ over AWGN channel, and Figure 18D illustrates the probability of a frame synchronization confirmation success P_S on downlink DPCCH with $N_{pilot}=4$ over AWGN between the pilot pattern of the preferred embodiment and the current pilot pattern, where P_D, P_{FA}, and P_S are given as a function of E_b/N_0 ratio (E_b = energy per bit, N_0 = noise power spectral density).

The P_D and P_S of the pilot patterns of the preferred embodiment are greater than that of current pilot pattern. Furthermore, the P_{FA} of the pilot patterns in accordance with the preferred embodiment are also smaller than that of the current pilot patterns. The theoretical equations (9) and (12) are identical to simulation results of Figure 18D. Therefore, there is significant difference between the frame synchronization performance of pilot patterns of the preferred embodiment and that of current pilot pattern. For example, from Figure 18D, there is 3dB gain at P_S = 0.93 by employing the pilot patterns of the preferred embodiment.

The frame synchronization words of the preferred embodiment are especially suitable for frame synchronization confirmation. By adding the autocorrelation functions of shaded frame synchronization words, double maximum values equal in magnitude and opposite polarity at zero and middle shifts are obtained. This property can be used to slot-by-slot and double-check frame synchronization timing and reduce the synchronization

search time. The performance of frame synchronization confirmation over AWGN using pilot pattern illustrate the significant differences between the frame synchronization performance of the pilot pattern of the preferred embodiment and the current pilot pattern.

First Embodiment of Downlink DPCH, PCCPCH and SCCPH for STTD Diversity

Figure 19A illustrates new pilot symbol patterns of Downlink DPCH for the diversity antenna using a space time block coding based transmit diversity (STTD). For the diversity pilot symbol pattern on downlink DPCH, STTD is applied to the shaded pilot symbols #1 and #3 for N_{pilot} = 8, and the shaded pilot symbols #1, #3, #5, and #7 for N_{pilot} = 16. The non-shaded pilot symbols #0 and #2 for N_{pilot} = 8 , and non-shaded pilot symbols #0, #2, #4,and #6 for N_{pilot} = 16 are encoded to be orthogonal to the pilot symbol of Figure 15A. However, the diversity pilot pattern for downlink DPCH with N_{pilot} = 4 are STTD encoded since STTD encoding requires two symbols. Figure 19B illustrates the mapping relationship between the 8 words C_1-C_8 of Figure 12A and shaded pilot symbol patterns of Figure 19A.

Figure 19C illustrates the new diversity antenna pilot symbol pattern for PCCPCH. The pilot symbols of Figure 19C are encoded to be orthogonal to the pilot symbols of Figure 16A. Figure 19D illustrates the mapping relationship between the words C_1-C_8 of Figure 12A and shadowed pilot symbol patterns of Figure 19C.

Figure 19E illustrates the new pilot symbol pattern for the diversity antenna when STTD encoding is used on the SCCPCH. For the diversity pilot symbol pattern on SCCPCH, STTD is applied to the shaded pilot symbols #1, and #3 of N_{pilot} = 8, and shaded pilot symbols #1, #3, #5 and #7 of N_{pilot} = 16 in Figure 19E, whereas the non-shaded pilot symbols #0 and #2 of N_{pilot} = 8, and non-shaded #0, #2, #4, #6 of N_{pilot} = 16 are encoded to be orthogonal to those of Figure 16C. Figure 19F illustrates the mapping relationship between the words C_1-C_8 of Figure 12A and shaded pilot symbol patterns of Figure 19E.

Since the above is based on words C_1-C_8, the previous discussion regarding the uplink DPCCH and downlink DPCH, PCCPCH and SCCPH is readily applicable. One of ordinary skill in the art can readily appreciate the features for downlink using diversity antenna based on previous disclosure, and a detailed disclosure is omitted.

Alternative Embodiments for Uplink DPCCH and Downlink DPCH and PCCPCH

Figure 20A is a table illustrating frame synchronization words C_1-C_{16} (i=16) and autocorrelated function in accordance with another preferred embodiment of the present invention. The frame synchronization words C_1-C_{16} can be classified into the PCSP of the first embodiment, as follows:

$$E = \{C_1, C_3, C_9, C_{11}\}$$

$$F = \{C_2, C_4, C_{10}, C_{12}\}$$

$G = \{C_5, C_7, C_{13}, C_{15}\}$

$H = \{C_6, C_8, C_{14}, C_{16}\}$

The classification of the alternative frame synchronization words C_1-C_{16} are also applicable to equations (1)-(6), and have the same properties and characteristics of the first embodiment. Figure 20B is a table illustrating the autocorrelation function of the pilot bits of each frame synchronization word classified in the PCSP. In this particular case, each class contains four sequences and the sequences of the same class have the same autocorrelation function.

Figure 20C illustrates the pilot bit pattern of uplink DPCCH with $N_{pilot}=6$ and 8 and Figure 20D illustrates a mapping relationship between the alternative frame synchronization words C_1-C_{16} of Figure 20A and the shaded frame synchronization words of Figure 20C. Figures 20E and 20F illustrate the pilot symbol pattern of downlink DPCH with 8, 16, 32, 64, 128, 256, 512, 1024, 2048 and 4096 ksps, and Figure 20G illustrates a mapping relationship between the alternative frame synchronization words C_1-C_{16} of Figure 20A and the shaded frame synchronization words of Figures 20E and 20F. Figure 20H illustrates the pilot symbol pattern of downlink PCCPCH and Figure 20I illustrates a mapping relationship between the alternative frame synchronization words C_1-C_{16} of Figure 20A and the shaded frame synchronization words of Figure 20H.

Since the above is based on alternative words C_1-C_{16}, which have the same features as the words C_1-C_8 of the first embodiment, the previous discussion regarding the uplink DPCCH and downlink DPCH, PCCPCH and SCCPH of the first embodiment is readily applicable. One of ordinary skill in the art can readily appreciate the features of this embodiment based on previous disclosure, and a detailed disclosure is omitted.

The frame synchronization words of the preferred embodiment are especially suitable for frame synchronization confirmation. By adding the autocorrelation functions of shaded frame synchronization words, double maximum values equal in magnitude and opposite polarity at zero and middle shifts are obtained. This property can be used to slot-by-slot and double-check frame synchronization timing and reduce the synchronization search time. Further the present invention allows a simpler construction of the correlator circuit for a receiver, thereby reducing the complexity of the receiver. Moreover, the present invention allows accurate establishment of the frame synchronization. Due to various advantages of the present invention, the first preferred embodiment has been accepted by the 3GPP, as shown in TS 25.211 v2.0.1, distributed June 1999, whose entire disclosure is hereby incorporated by reference therein.

Preferred Embodiment for L=15

The above pilot patterns in accordance with preferred embodiments of the present invention have various advantages including frame synchronization

confirmation. In the above preferred embodiments, the physical channel of the up-link or down-link has a chip ratio of 4.096Mcps, which results from the use of a pilot pattern based on a length of 16 slots for the frame synchronization. In other words, the chip ratio is based on a slot length of 2^n. However, if the chip ratio changes from 4.096Mcps to 3.84Mcps, alternative pilot patterns are needed since one radio frame is based on a slot length of 15 slots. Hence, alternative pilot patterns are needed for 15 slots (L=15) due to OHG harmonization.

Figure 21 illustrates a preferred embodiment for the new frame synchronization words C_1-$C_{i\text{-th}}$, which has the auto-correlation function of lowest out-of-phase coefficient and the lowest magnitude of cross-correlation function with minus peak value at middle shift, where i=8. The frame synchronization words are used to design the regular pilot patterns and diversity antenna pilot patterns of uplink DPCH, and downlink DPCH and SCCPCH of the preferred embodiment. By using the two correlation functions, it is possible to double check frame synchronization at zero and middle shifts. When performance evaluation of single-check and double-check frame synchronization confirmation is carried out over AWGN environment, the words C_1-C_8 of Figure 21 are suitable for frame synchronization confirmation

The frame synchronization words C_1-C_8 have the following two-valued auto-correlation function:

$$R_i(\tau)=\begin{cases}15, & \tau=0\\ -1, & \tau\neq 0\end{cases},\quad i=1,2,\cdots,8 \tag{13}$$

where $R_i(\tau)$ is the auto-correlation function of frame synchronization word C_i. Similar to L=16, the words of Figure 21 can be divided into 4 classes, as follows:

$$E = \{C_1, C_2\}$$

$$F = \{C_3, C_4\}$$

$$G = \{C_5, C_6\}$$

$$H = \{C_7, C_8\}$$

The two words within the same class are PCSP. The cross-correlation spectrum for the preferred pair $\{C_1, C_2\}$, $\{C_3, C_4\}$, $\{C_5, C_6\}$, or $\{C_7, C_8\}$ is

$$R_{i,j}(\tau)=\begin{cases}-15, & \tau=7\\ 1, & \tau\neq 7\end{cases} \tag{14}$$

$$R_{j,i}(\tau+1)=\begin{cases}-15, & \tau=7\\ 1, & \tau\neq 7\end{cases} \tag{15}$$

where $R_{i,j}(\tau)$ is cross-correlation function between two words of preferred pair of E, F, G, H, and i, j = 1, 2, 3, ..., 8. By combining such auto-correlation and cross-correlation functions, the following equations (16) and (17) are obtained:

$$\sum_{i=1}^{\alpha} R_i(\tau) = \begin{cases} \alpha \cdot 15, & \tau = 0 \\ -\alpha, & \tau \neq 0 \end{cases}, \quad \alpha = 1,2,3,...,8 \tag{16}$$

$$\sum_{i=1}^{\alpha/2} (R_{2i-1,2i}(\tau) + R_{2i,2i-1}(\tau+1)) = \begin{cases} -\alpha \cdot 15, & \tau = 7 \\ \alpha, & \tau \neq 7 \end{cases}, \quad \alpha = 2,4,6,8 \tag{17}$$

From equations (16) and (17), when $\alpha=2$, Figure 22A illustrates the addition of two auto-correlation functions, and Figure 22B illustrates the addition of two cross-correlation functions between the two frame synchronization words within the same class. Similarly, from equations (16) and (17), when $\alpha=4$, Figure 22C illustrates the addition of four auto-correlation functions, and Figure 22D illustrates the addition of four cross-correlation functions between the four frame synchronization words of two classes E and F.

Since the auto-correlation function of the frame synchronization words C_1-C_8 in accordance with this preferred embodiment has the lowest out-of-phase coefficient, single-check frame synchronization confirmation is feasible by applying the positive threshold value at (a) of the auto-correlation function output of Figure 22C. Furthermore, double-check frame synchronization confirmation is also achieved by setting the negative threshold value at (b) of the cross-correlation function output of Figure 22D.

Figures 23A illustrates the pilot bit patterns on uplink DPCCH with N_{pilot} = 2, 3, and 4, and Figure 23C illustrates the pilot bit patterns on uplink DPCCH with N_{pilot} = 2,3, and 4 in accordance with an alternative embodiment compared to Figure 23A. Further, Figures 23E and 23F illustrate the pilot bit patterns on uplink DPCCH with

N_{pilot} = 5, 6, 7, and 8. The shaded parts of Figures 23A, 23C, 23E and 23F can be used for frame synchronization words, and the value of pilot bit other than the frame synchronization word is 1. Figures 23B and 23D illustrate the mapping relationship between the frame synchronization words of Figure 21, and shaded frame synchronization words of Figures 23A and 23D, respectively. Further, Figure 23G illustrates the mapping relationship between the frame synchronization words of Figure 21, and the shaded frame synchronization words of Figures 23E and 23F.

The various description of above for uplink DPCCH when L=16 is readily applicable to this preferred embodiment when L=15, including the correlator circuits (with some modifications) and the generally characteristics. For example, as shown in frame synchronization words C_1-C_8 of Figure 21, each word has substantially the same number of 1 and 0. In this preferred embodiment, the result of b_1-b_0 is plus or minus one, e.g., close to zero. Further, when the number of slots is 15, i.e., odd, the result of b_3-b_4 equals plus or minus one, e.g., close to zero. Further, since two frame synchronization words are used for N_{pilot} = 2, 3, and 4 and there are fifteen timeslots in a radio frame, the number of pilot bits used for synchronization is 30 per frame. For N_{pilot} = 5, 6, 7 and 8, since four synchronization words are used for fifteen timeslots in a radio frame, the number of pilot bits used for synchronization is 60 per frame. Moreover, the result of the addition of two or four auto-correlation functions and cross-correlation functions between two or four frame synchronization words corresponds to Figures 22A-22D.

With the implementation of the novel pilot patterns, the values for the number of bits per field are shown below in Table 5 and Table 6 with reference to Figure 4. The channel bit and symbol rates given in Table 5 are the rates immediately before spreading.

Table 5: DPDCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
15	15	256	150	10	10
30	30	128	300	20	20
60	60	64	600	40	40
120	120	32	1200	80	80
240	240	16	2400	160	160
480	480	8	4800	320	320
960	960	4	9600	640	640

There are two types of Uplink Dedicated Physical Channels; those that include TFCI(e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of Table 6. The channel bit and symbol rates given in Table 6 are the rates immediately before spreading.

Table 6: DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{pilot}	N_{TPC}	N_{TFCI}	N_{FBI}
15	15	256	150	10	6	2	2	0
15	15	256	150	10	8	2	0	0
15	15	256	150	10	5	2	2	1
15	15	256	150	10	7	2	0	1

15	15	256	150	10	6	2	0	2
15	15	256	150	10	5	1	2	2

The Random Access Channel (RACH) is an uplink transport channel that is used to carry control information from the UE. The RACH may also carry short user packets. The RACH is always received from the entire cell. Figure 23H illustrates the structure of random access channel. The 10 ms message is split into 15 slots, each of length T_{slot} = 2560 chips. Each slot has two parts, a data part that carries Layer 2 information and a control part that carries Layer 1 control information. The data and control parts are transmitted in parallel.

The data part includes $10*2^k$ bits, where k=0,1,2,3. This corresponds to a spreading factor of 256, 128, 64, and 32 respectively for the message data part. The control part has 8 known pilot bits to support channel estimation for coherent detection and 2 bits of rate information. This corresponds to a spreading factor of 256 for the message control part.

With the implementation of the novel pilot patterns, the values for the number of bits per field are shown in Table 7 with reference to Figure 23H.

Table 7: Random-access message data fields.

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}
15	15	256	150	10	10
30	30	128	300	20	20
60	60	64	600	40	40
120	120	32	1200	80	80

Figure 23I illustrates the random access message control fields and there is always 8 pilot symbols per slot for channel estimation. Due to the unique characteristics of the frame synchronization words in accordance with the preferred embodiment, the frame synchronization words C_1-C_8 can be used in the pilot bit pattern of the RACH for channel estimation. Figure 23J illustrates the pilot bit pattern of the RACH, and the mapping relationship is the same as the mapping relationship illustrated in Figure 23G for $N_{pilot}=8$. Due to the novel characteristics of the frame synchronization words C_1-C_8, which can also be used solely for channel estimation, it is easy to reuse the pilot patterns, which allows commonality between different uplink channels.

Figure 24A illustrates the pilot symbol patterns on downlink DPCH when N_{pilot} = 2, 4, 8, and 16. The shaded parts of Figure 24A can be used for frame synchronization symbols, each symbol having one frame synchronization word for the I channel branch and another frame synchronization word for the Q channel branch, and the value of pilot symbol other than the frame synchronization word is 11. Figure 24B illustrates the

mapping relationship between the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 24A.

Figure 24C illustrates the pilot symbol patterns of downlink DPCH for the diversity antenna using STTD. For the diversity pilot symbol pattern on downlink DPCH, STTD is applied to the shaded pilot symbols #1 and #3 for N_{pilot}=8, and #1, #3, #5, and #7 for N_{pilot} = 16. The non-shaded pilot symbols of #0 and #2 for N_{pilot} = 8 and 0#, #2, #4 and #6 for N_{pilot} = 16 are encoded to be orthogonal to the pilot symbol of Figure 24A. However, the diversity pilot pattern for downlink DPCH with N_{pilot} = 4 are STTD encoded since STTD encoding requires two symbols. Since the STTD encoded pilot symbol pattern is orthogonal to ordinary pilot symbol pattern, the STTD encoded pilot pattern can also be used for antenna verification of feedback mode diversity. Figure 24D illustrates the mapping relationship between the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 24C.

With the implementation of the novel pilot patterns, the below Table 8 shows the number of bits per slot of the various fields with reference to Figure 8. There are basically two types of downlink Dedicated Physical Channel; those that include TFCI (e.g. for several simultaneous services) and those that do not include TFCI(e.g. for fixed-rate services). These types are reflected by the duplicated rows of Table 8. The channel bit and symbol rates given in Table 8 are the rates immediately before spreading. If there is no TFCI, then the TFCI field is left blank (*).

Table 8: DPDCH and DPCCH fields

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/Frame			Bits/ Slot	DPDCH Bits/Slot		DPCCH Bits/Slot		
			DPDCH	DPCCH	TOT		N_{Data1}	N_{Data2}	N_{TFCI}	N_{TPC}	N_{Pilot}
15	7.5	512	60	90	150	10	2	2	0	2	4
15	7.5	512	30	120	150	10	0	2	2	2	4
30	15	256	150	150	300	20	2	8	0	2	8
30	15	256	120	180	300	20	0	8	2	2	8
60	30	128	450	150	600	40	6	24	0	2	8
60	30	128	420	180	600	40	4	24	2	2	8
120	60	64	900	300	1200	80	4	56	8*	4	8
240	120	32	2100	300	2400	160	20	120	8*	4	8
480	240	16	4320	480	4800	320	48	240	8*	8	16
960	480	8	9120	480	9600	640	112	496	8*	8	16
1920	960	4	18720	480	19200	1280	240	1008	8*	8	16

Figure 25A illustrates the pilot symbol patterns for downlink SCCPCH for N_{pilot} = 8 and 16, and Figure 25B illustrates the mapping relationship of the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 25A. Further, Figure 25C illustrates the pilot symbol patterns of downlink SCCPCH for Npilot = 8 and 16 for the diversity antenna using STTD, and Figure 25D illustrates the mapping relationship between the frame synchronization words C_1-C_8 of Figure 21 and shaded pilot symbol patterns of Figure 25C.

With the implementation of the novel pilot patterns, the values for the number of bits per field are given in Table 9 with reference to Figure 11B. The channel bit and

symbol rates given in Table 9 are the rates immediately before spreading. In the Secondary Common Control Physical Channel, it is possible to have burst transmission based on radio frame units. When burst transmission is performed, pilot symbols shall be added to the head of the burst. The number of symbols and the symbol pattern of the pilot symbols to be attached shall take the pattern of Slot #15.

Table 9: Secondary CCPCH fields with pilot bits

Channel Bit Rate (kbps)	Channel Symbol Rate (ksps)	SF	Bits/ Frame	Bits/ Slot	N_{data}	N_{pilot}	N_{TFCI}
30	15	256	300	20	12	8	0
30	15	256	300	20	10	8	2
60	30	128	600	40	32	8	0
60	30	128	600	40	30	8	2
120	60	64	1200	80	72	8	0
120	60	64	1200	80	64	8	8
240	120	32	2400	160	152	8	0
240	120	32	2400	160	144	8	8
480	240	16	4800	320	304	16	0
480	240	16	4800	320	296	16	8
960	480	8	9600	640	624	16	0
960	480	8	9600	640	616	16	8
1920	960	4	19200	1280	1264	16	0
1920	960	4	19200	1280	1256	16	8

As can be appreciated, the various description of above for downlink DPCH when L=16 is readily applicable to this preferred embodiment when L=15, including the correlator circuits (with some modifications) and the generally characteristics. Moreover,

the result of the addition of two or four auto-correlation functions and cross-correlation functions between two or four frame synchronization words corresponds to Figures 22A-22D.

In order to evaluate the performance of the frame synchronization words in accordance with the preferred embodiment for 15 slots per frame, the following events and parameters are first defined:

H_1 : The event that the auto-correlator output exceeds the predetermined threshold at zero slot offset.

H_2 : The event that the auto-correlator output exceeds the predetermined threshold at zero slot offset or the cross-correlator output is smaller than $-1\times$(predetermined threshold) at 7 slot offset.

H_3 : The event that the auto-correlator exceeds the predetermined threshold at slot offset except zero.

H_4 : The event that the cross-correlator output is smaller than $-1\times$(predetermined threshold) at slot offset except 7.

P_S : Probability of a frame synchronization confirmation success.

P_{FA} : Probability of a false alarm.

The frame synchronization is confirmed if the output of the correlator using the frame synchronization word exceeds the predetermined threshold. The success of the frame synchronization confirmation is determined when the successive S_R frame synchronization is confirmed. Otherwise, the frame synchronization confirmation failure

is determined. Thus, the probability of a frame synchronization confirmation success is defined by

$$P_S = \begin{cases} (\mathrm{Prob}(H_1))^{S_R}, & \text{single check} \\ (\mathrm{Prob}(H_2))^{S_R}, & \text{double check} \end{cases} \tag{18}$$

The probability of a false alarm can be expressed as

$$\begin{aligned} P_{FA} &= \mathrm{Prob}(H_3) \\ &= \mathrm{Prob}(H_4) \end{aligned} \tag{19}$$

The parameters of Figure 26A are used to evaluate the performance of the pilot bit pattern on uplink DPCCH over AWGN. Figure 26B illustrates the probability of frame synchronization confirmation success P_S on uplink DPCCH with $N_{pilot} = 6$ over AWGN channel. Further, Figure 26C illustrates the probability of a false alarm P_{FA} on uplink DPCCH with $N_{pilot} = 6$ over AWGN channel. The P_S and P_{FA} are given as a function of E_b/N_0 ratio (E_b = energy per bit, N_0 = noise power spectral density).

The P_S of single-check and double-check frame synchronization confirmation with $S_R = 3$ on uplink DPCCH is smaller than 0.945 and 0.99 at -5dB, respectively. Further, about 4dB gain is obtained by employing double-check method compared to single-check method. From Figure 26C, the probability of a false alarm with normalized threshold =

0.6 at -5dB is smaller than 2.5×10^{-4}. The pilot pattern can be used for frame synchronization confirmation since perfect frame synchronization confirmation success with zero false alarm was detected at Eb/No = 0dB when double-check frame synchronization confirmation method was used.

Figure 27 is a comparision chart between the embodiments for 15 timeslots and 16 slots. Including the various advantages for L=16, the pilot bit/symbol patterns for L=15 in accordance with the preferred embodiment have additional advantages. By using this property/characteristics of the frame synchronization words, double-check frame synchronization scheme can be obtained. There is significant gain about 4dB by employing the double-check frame synchronization confirmation method compared to single-check method. However, in the case of 15 slots, the complexity of the correlator circuit is doubled since an auto-correlator for positive peak detection and a cross-correlator for negative peak detection are used.

Since the auto-correlation function of the frame synchronization words of the 15 slots has the lowest out-of-phase coefficient, the single-check frame synchronization confirmation method can also be employed; whereas, in the case of 16 slots, there is some problems due to +4 or -4 out-of-phase coefficients. The pilot patterns of 15 slots is very suitable for frame synchronization confirmation since perfect frame synchronization confirmation success with zero false alarm was detected at Eb/No = 0dB on uplink DPCH when double-check frame synchronization confirmation method was used. Due

to the various advantageous of the preferred embodiment, the pilot bit/symbol patterns of 15 slots have been again accepted by the 3GPP.

STTD Encoding for Downlink

The 3GPP RAN has a description in TS s1.11 v1.1.0 on a downlink physical channel transmit diversity on application of a open loop transmit diversity and a closed loop transmit diversity in different downlink physical channels. The open loop transmit diversity uses STTD encoding based on spatial or temporal block coding. As described above, the present invention suggest new downlink pilot patterns using the STTD encoding into consideration. The STTD encoding is used optionally at the base station and preferably required at the user equipment.

Figure 28A illustrates a block diagram of an STTD transmitter 60 according to the 3GPP RAN standards for open loop transmit diversity. A data provided to the STTD transmitter in a non-diversity mode passes through a channel encoder 61 for channel coding, a rate matcher 62 for rate matching, and an interleaver 63 for interleaving, and therefrom to a first multiplexer 64. The multiplexer 64 multiplexes a final interleaved data, a TFCI field, and a TPC field. The STTD encoder 65 provides data patterns to be respectively transmitted through a first transmission antenna 67 and a second transmission antenna 68 to a second multiplexer 66. In other words, the second multiplexer 66 has symbols S_1 and S_2 by QPSK provided thereto together with symbols $-S_2^*$ and S_1^* produced to be orthogonal to the symbols S_1 and S_2.

Figure 28B explains an STTD encoding of an STTD transmitter 60 according to the 3 GPP RAN standards. For example, it is assumed that QPSK symbols provided to the STTD encoder 65 is "S_1=1 1" in a first symbol period 0 T, and "S_2= 1 0" in a second symbol period T 2T. The symbols produced to be orthogonal to the QPSK symbols at the STTD encoder 65 is "0 0" in the first symbol period 0 T, and "1 0" in the second symbol period T 2T.

The symbols produced according to the STTD encoding have the following characteristics. The symbols "0 0" produced in the first symbol period 0 T are symbols converted from QPSK symbols S_2 in the second symbol period T 2T provided to the STTD encoder 65, and the symbols "1 0" produced in the second symbol period T 2T are symbols converted from the QPSK symbols S_1 in the first symbol period 0 T provided to the STTD encoder 65.

The symbols "$-S_2^*$ and S_1^*" are produced in respective symbol periods through shifting, complementary and conversion process according to the STTD encoding. Eventually, since the symbols "$-S_2^*$ and S_1^* = 0 0, 1 0" and the QPSK symbols S_1 and S_2 = 1 1, 1 0 provided to the STTD encoder 65 have correlation values "0", they are orthogonal to each other.

The STTD encoded pilot symbol patterns of Figure 19A are orthogonal to the pilot symbol patterns of Figure 15A and a method for producing the pilot symbol patterns of Figure 19A by applying the STTD encoding principle to the pilot symbol

patterns of Figure 15A will be explained with reference to Figure 28B.

The STTD encoding is preferably carried out in units of two symbols as bundles. In other words, if it is assumed that the two symbols are "$S_1=A+jB$" and "$S_2=C+jD$", the STTD encoding is carried out with S_1 and S_2 tied as a unit. In this instance, "A" and "C" are pilot bits for the I channel branch and "B" and "C" are pilot bits for the Q channel branch. An STTD encoding of "S_1 S_2"produces "$-S_2^*$ S_1^*" (where * denotes a conjugate complex). At the end of the encoding, the STTD encoded two symbols will be "$-S_2^*=-C+jD$" and "$S_1^*=A-jB$".

Specifically, when the symbol rate is 8ksps ($N_{pilot}=4$) of Figure 15A, "$S_1=1+j$, $S_2=C_1+jC_2$" of respective symbol #0 and symbol #1 are STTD encoded into "$-S_2^*=-C_1+jC_2$" of symbol #0 and "$S_1^*=1-j0$" of symbol #1. When symbol rate is 16, 32, 64 or 128ksps (Npilot=8) in Figure 15A, "$S_1=C_1+jC_2$, $S_2=C_3+jC_4$" at symbol #1 and symbol #3 are STTD encoded into "$-S_2^*=-C_3+jC_4$" of symbol #1 and "$S_1^*=C_1-jC_2$" of symbol #3 of Figure 19A. The non-shaded symbol #0 and symbol #2 in Figure 19A are made orthogonal to the non-shaded symbol #0 and symbol #2 in Figure 15A. In other words, "11", "11" in Figure 15A are made to be "11", "00" in Figure 19A.

When the symbol rate is 256, 512, 1024ksps ($N_{pilot}=16$), there are four shaded pilot symbols. Therefore, the pilot symbols are STTD encoded by two shaded symbols, e.g., "$S_1=C_1+jC_2$, $S_2=C_3+jC_4$" of shaded symbol #1 and symbol #3 of Figure 19A, are STTD encoded into "$-S_2^*=-C_3+jC_4$" of symbol #1 and "$S_1^*=C_1-jC_2$" of symbol #3 of Figure 19A,

and "$S_1=C_5+jC_6$, $S_2=C_7+jC_8$" of a third and a fourth shaded symbol #5 and symbol #7 of Figure 15A, are STTD encoded into "$-S_2^*=-C_7+jC_8$" of symbol #5 and "$S_1^*=C_5-jC_6$" of symbol #7 of Figure 19A. The non-shaded symbol #0, symbol #2, symbol #4, and symbol #6 of Figure 19A, are orthogonal to the non-shaded symbol #0, symbol #2, symbol #4, and symbol #6 of Figure 15A. That is, "11", "11", "11", "11" of Figure 15A are made into "11", "00", "11", "00" of Figure 19A.

The symbols of Figure 19A which is produced by applying the STTD encoding to the pilot symbol patterns in Figure 15A have the following characteristics. In Figure 15A, when the symbol rate is 8ksps ($N_{pilot}=4$), 16, 32, 64, or 128ksps ($N_{pilot}=8$), or 256, 512, or 1024ksps ($N_{pilot}=16$), the shaded column sequences are classed into four PCSP 'E', 'F', 'G' or 'H' starting from the lowest symbol number, and the column sequences comprises words C_1, C_2, C_3, and C_4 and C_5, C_6, C_7, and C_8 in accordance with the preferred embodiment in an order corresponding to the classes, to express each PCSP as $E=\{C_1, C_5\}$, $F=\{C_2, C_6\}$, $G=\{C_3, C_7\}$, and $H=\{C_4, C_8\}$, as described above. Since the pilot symbol patterns of Figure 19A are the pilot symbol patterns in Figure 15A after the STTD encoding, when the symbol rate is 256, 512, or 1024ksps ($N_{pilot}=16$), the column sequences are arranged in "$-C_3$, C_4, C_1, and $-C_2$" and "$-C_7$, C_8, C_5, $-C_6$" when the shaded column sequences are classed in 'E', 'F', 'G' and 'H' starting from the lowest symbol number. Hence, $E=\{-C_3, -C_7\}$, $F=\{C_4, C_8\}$, $G=\{C_1, C_5\}$, and $H=\{-C_2, -C_6\}$. Compare Figures 15B and 19B.

As per the non-shaded pilot symbol patterns, when each slot has 4 pilot bits, "10" is allocated to all slots of symbol #1. When each slot has 8 pilot bits, "11" is allocated to all slots of symbol #0, and "00" to all slots of symbol #2. When each slot has 16 pilot bits, "11" is allocated to all slots of symbol #0, "00" to all slots of slot #2, "11" is allocated to all slots of symbol #4, and "00" to all slots of symbol #6. Accordingly, cross correlation of the non-shaded symbols of Figure 19A, i.e., the column sequences having "10(N_{pilot}=4 bits)", "11(N_{pilot}=8 bits and N_{pilot}=16 bits)", or "00(N_{pilot}-8 bits and N_{pilot}=16 bits)", with the shaded column sequences have values "0" for all time shifts " ". Further, when a slot has 4, 8, or 16 pilot bits, the present invention arranges the pilot symbol patterns such that a cross correlation of a word of I channel branch and a word of a Q channel branch in every symbol number is "0" at a time shift "τ=0".

The above description of STTD encoding is readily applicable to downlink PCCPCH (compare Figures 16A and 19C) and downlink Secondary CCPCH (compare Figures 16C and 19E) for 16 slots. Further, the STTD encoding is readily applicable to downlink DPCH (compare Figures 24A and 24C) and downlink SCCPCH (compare Figures 25A and 25C) for 15 slots.

Alternative Embodiments of Uplink and Downlink Apparatus for Frame Synchronization

The frame synchronization words of Figure 21 are used for the frame synchronization detection, in case of using 15 slots per frame. To use the frame

synchronization words of Figure 21 for the frame synchronization detection, the following arrangement features are preferable.

The number of bit values '0' or '1' is greater by 1 than the number of bit values '1' or '0' in each code sequence C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8 to allow (1) the correlation value between the pilot sequences at all delay time points to be a minimum value when the pilot sequence all having the bit value '1' is inserted between the shaded sequences of uplink and dowlink, and (2) the pilot sequences to have the minimum correlation value between the pilot sequences at all delay time points or time shifts when the code sequence all having the bit value '0' is inserted between the pilot sequences C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8.

Further, each pilot sequences C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8 are designed to have the minimum correlation value between the pilot sequences (for example, C_1 and C_2, C_2 and C_3,...) adjacent to each other at the delay time point of '0'. The pilot sequences C_5, C_6, C_7 and C_8 are formed by the shifting of the pilot sequences C_1, C_2, C_3 and C_4. In other words, the pilot sequences C_5, C_6, C_7 and C_8 are formed by shifting the pilot sequences C_1, C_2, C_3 and C_4, have the minimum correlation value between the pilot sequences adjacent to each other at the delay time point of '0'.

Each pilot sequence C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8 is designed to have the minimum correlation value at any delay time point except at the delay time point of '0'.

The correlation value between the pilot sequences C_1 and C_2 has a maximum value having a negative polarity at an intermediate delay time point, and the correlation value between the pilot sequences C_2 and C_1 has a minimum value at any delay time point except at the intermediate delay time point. The correlation value between the pilot sequences C_3 and C_4 has a maximum value having a negative polarity at an intermediate delay time point, and the correlation value between the pilot sequences C_4 and C_3 has a minimum value at any delay time point except at the intermediate delay time point.

The correlation value between the pilot sequences C_5 and C_6 has a maximum value having a negative polarity at an intermediate delay time point, and the correlation value between the pilot sequences C_6 and C_5 has a minimum value at any delay time point except at the intermediate delay time point. The correlation value between the pilot sequences C_7 and C_8 has a maximum value having a negative polarity at an intermediate delay time point, and the correlation value between the pilot sequences C_8 and C_7 has a minimum value at any delay time point except at the intermediate delay time point.

Particularly, the pilot sequence C_1 is shifted and inverted to generate the pilot sequence C_2. The pilot sequence C_3 is shifted and inverted to generate the pilot sequence C_4. The pilot sequence C_5 is shifted and inverted to generate the pilot sequence C_6. The pilot sequence C_7 is shifted and inverted to generate the pilot sequence C_8.

The frame synchronization words of Figure 21 are designed based upon the above

arrangement characteristics for use frame synchronization detection of uplink and downlink channels, and particularly, for double checking the frame synchronization detection.

As appreciated from the above arrangement characteristics, each pilot sequence of the frame synchronization words exhibits a self-correlation feature as follows:

$$R_{Ci}(\tau) = \begin{pmatrix} 15, \tau = 0 \\ -1, \tau \neq 0 \end{pmatrix} \tag{20}$$

where i = 1, 2, 3,..., 8, and $R_{Ci}(\tau)$ represents self-correlation functions of each pilot sequence C_1 to C_8. As described above, the words are divided into PCSP of E, F, G and H.

The pairs of pilot sequences {Ci, Cj} contained in the same class, e.g. {C_1, C_2}, {C_3, C_4}, {C_5, C_6}, and {C_7, C_8} have the cross-correlation characteristic as follows:

$$R_{C_j, C_i}(\tau + 1) = \begin{pmatrix} -15, \tau = 7 \\ 1, \tau \neq 7 \end{pmatrix} \tag{21}$$

where i = 1 & j = 2, i = 3 & j = 4, i = 5 & j = 6, and i = 7 & j = 8.

$$R_{C_j, C_i}(\tau + 1) = \begin{pmatrix} -15, \tau = 7 \\ 1, \tau \neq 7 \end{pmatrix} \tag{22}$$

where j = 2 & i = 1, j = 4 & i = 3, j = 6 & i = 5, and j = 8 & i = 7.

In equation (21), $R_{Ci,Cj}(\tau)$ represents a cross-correlation function between the pair of code sequences in each class. In equation (22), $R_{Cj,Ci}(\tau+1)$ is a function of the cross-correlation of the code sequence C_i with the code sequence C_j shifted by a length of bit '1'.

The combination of the self-correlation feature of equation (20) with the cross-correlation feature of the equations (21) and (22) is given by the following:

$$\sum_{i=1}^{\alpha} R_{C_i}(\tau) = \begin{pmatrix} \alpha \cdot 15, \tau = 0 \\ -\alpha, \tau \neq 0 \end{pmatrix} \tag{23}$$

where α = 1, 2, 3, ..., 8.

$$\sum_{i=1}^{\alpha/2} [R_{C_{2i-1}, C_{2i}}(\tau) + R_{C_{2i}, C_{2i-1}}(\tau+1)] = \begin{pmatrix} -\alpha \cdot 15, \tau = 7 \\ \alpha, \tau \neq 7 \end{pmatrix} \tag{24}$$

where α = 2, 4, 6, 8.

Figures 29A and 29B are graphs illustrating an embodiment of correlation results using a pilot pattern in accordance with a preferred embodiment and Figures 30A and 30B

are graphs illustrating another embodiment of correlation results using a pilot pattern in accordance with a preferred embodiment.

The correlation results in Figures 29A to 30B are obtained from the equations (23) and (24), where Figures 29A and 29B show the correlation results when $\alpha = 2$ in equations (23) and (24) and Figures 30A and 30B shows the correlation results when $\alpha = 4$ in equations (23) and (24).

In more detail, Figure 29A shows the added result of the self-correlation functions when $\alpha = 2$ in equation (23), and Figure 29B shows the added result of the cross-correlation functions when $\alpha = 2$ in equation (24). Figure 30 shows the added result of the self-correlation functions when $\alpha = 4$ in equation (23) and Figure 30B shows the added result of the cross-correlation functions when $\alpha = 4$ in equation (24).

With the observation of each correlation result in Figures 29A to 30B, a single check is executed upon the frame synchronization detection, and with the concurrent observation of the self-correlation and cross-correlation results in Figures 29A to 30B, a double check is executed upon the frame synchronization detection. Based on the above, the pilot patterns and pilot symbols of L=15, as described above, for uplink and downlink are generated.

The frame synchronization words, preferably, 8 words, of Figure 21 are generated from a single pilot sequence. The relationship between the frame synchronization words

is given by the following equation (25). In more detail, the relationship between the pilot sequence C_1 and the other pilot sequences is given.

$$\begin{aligned} C_1(t+j+\tau) &= -C_2(t+j+\tau+7) \\ &= C_3(t-j-\tau+5) \\ &= -C_4(t-j-\tau+12) \\ &= C_5(t+j+\tau+10) \\ &= -C_6(t+j+\tau+2) \\ &= C_7(t-j-\tau) \\ &= -C_8(t-j-\tau+7) \end{aligned} \quad (25)$$

In equation (25), the pilot sequence C_1 is generated by inverting, cyclic shifting, or reversing the other code sequences.

Based upon equation (25), when $\alpha = 8$ in equation (23), the added result of the self-correlation functions is given by the following equation (27). Before calculating the added result, however, the sum (S) of the eight pilot sequences should be obtained by equation (26):

$$\begin{aligned} S(t+j+\tau) = {} & C_1(t+j+\tau) - C_2(t+j+\tau+7) + C_3(t-j-\tau+5) \\ & -C_4(t-j-\tau+12) + C_5(t+j+\tau+10) - C_6(t+j+\tau+2) \\ & +C_7(t-j-\tau) - C8(t-j-\tau+7) = 8C_1(t+j+\tau) \end{aligned} \quad (26)$$

By using equation (26), equation (23) can be expressed as equation (27), in case of $\alpha = 8$.

$$\sum_{i=1}^{8} R_{C_i}(\tau) = \sum_{i=1}^{8}\sum_{j=0}^{14} C_i(t+j)\, C_i(t+j+\tau)$$

$$= \sum_{j=0}^{14} C_1(t+j)\cdot [C1(t+j+\tau) - C2(t+j+\tau+7) + C3(t-j-\tau+5)$$

$$-C4(t-j-\tau+12) + C5(t+j+\tau+10) - C6(t+j+\tau+2)$$

$$+ C7(t-j-\tau) - C8(t-j-\tau+7)]$$

$$= \sum_{j=0}^{14} C_1(t+j)\cdot S(t+j+\tau) \qquad (27)$$

Assuming that the pilot sequences C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_8 are defined by following equation (28), the index processed relation of equation (29) is given from equation (25).

$$C_1 = (C_{1,0}, C_{1,1}, \ldots, C_{1,14})$$

$$C_2 = (C_{2,0}, C_{2,1}, \ldots, C_{2,14})$$

$$C_3 = (C_{3,0}, C_{3,1}, \ldots, C_{3,14})$$

$$C_4 = (C_{4,0}, C_{4,1}, \ldots, C_{4,14})$$

$$C_5 = (C_{5,0}, C_{5,1}, \ldots, C_{5,14})$$

$$C_6 = (C_{6,0}, C_{6,1}, \ldots, C_{6,14})$$

$$C_7 = (C_{7,0}, C_{7,1}, \ldots, C_{7,14})$$

$$C_8 = (C_{8,0}, C_{8,1}, \ldots, C_{8,14}) \qquad (28)$$

$$
\begin{aligned}
C_{1',(j+\tau)(mod15)} &= -C_{2',(j+\tau+7)(mod15)} \\
&= C_{3',(-j-\tau+5)(mod15)} \\
&= -C_{4',(-j-\tau+12)(mod15)} \\
&= C_{5',(j+\tau+10)(mod15)} \\
&= -C_{6',(j+\tau+2)(mod15)} \\
&= C_{7',(-j-\tau)(mod15)} \\
&= -C_{8',(-j-\tau+7)(mod15)}
\end{aligned}
\tag{29}
$$

By using the above, a correlation processing apparatus for the frame synchronization according to the present invention is embodied. In the correlation processing apparatus of the present invention, the eight frame synchronization words are stored in a memory, and at this time, if the index (i, j) of each pilot sequence represents a memory address, the relation between the frame synchronization words stored in the memory is based on equation (29)

Figure 31 illustrates the correlation processing apparatus for the uplink channel in accordance with a preferred embodiment of the present invention, in which a single check for each slot is executed upon the frame synchronization detection.

As an example, the number of pilot bits N_{pilot} is 6 and the number of pilot sequences inputted for the frame synchronization detection is 4 in the correlation

apparatus of Figure 31. In other words, $\alpha = 4$, so the pilot sequences C_1 to C_4 of Figure 21 are used.

Hence, the equation (27) is transformed into the following equation (30):

$$\sum_{i=1}^{4} R_{C_i}(\tau) = \sum_{i=1}^{4}\sum_{j=0}^{14} C_i(t+j)\,C_i(t+j+\tau)$$
$$= \sum_{j=0}^{14} C_1(t+j)\cdot [C1(t+j+\tau) - C2(t+j+\tau+7) + C3(t-j-\tau+5) - C4(t-j-\tau+12)] \quad (30)$$

Since the characteristics of the frame synchronization words as indicated in equation (30) are utilized in the present invention, the correlation processing apparatus of Figure 31 implements a single correlator for the frame synchronization detection.

A signal in one frame unit of the uplink dedicated physical control channel is received, and the demodulated column sequences of the bit#1, bit#2, bit#4 and bit#5 in the pilot pattern of Figure 23E are inputted in the order of the slot number.

The four column sequences are inputted to a memory mapping/addressing block, in which the column sequences are stored in the frame unit and shifted and reversed by using the cross-correlation between the frame synchronization words of equation (29). In this case, the column sequences stored in the frame unit are given by the following equation (31). At this time, the index (i, j) of each column sequence represents the

memory address.

$$\hat{C}_1 = (\hat{C}_{1,0}, \hat{C}_{1,1}, \ldots, \hat{C}_{1.14})$$
$$\hat{C}_2 = (\hat{C}_{2,0}, \hat{C}_{2,1}, \ldots, \hat{C}_{2.14})$$
$$\hat{C}_3 = (\hat{C}_{3,0}, \hat{C}_{3,1}, \ldots, \hat{C}_{3.14})$$
$$\hat{C}_4 = (\hat{C}_{4,0}, \hat{C}_{4,1}, \ldots, \hat{C}_{4.14}) \qquad (31)$$

Each column sequence in equation (31) is shifted and reversed by the memory mapping/addressing block and then outputted. The outputs from the memory mapping/addressing block are added to provide the result value 'S1' as indicated by equation (32) to the correlator.

$$S1 = \hat{C}_{1',(j+\tau)(mod15)} - \hat{C}_{2',(j+\tau+7)(mod15)} + \hat{C}_{3',(-j-\tau+5)(mod15)} - \hat{C}_{4',(-j-\tau+12)(mod15)} \qquad (32)$$

The correlator correlates the previously stored pilot sequence C_1 and the result value 'S1' in equation (32) to thereby detect the frame synchronization. At this time, the correlated result is shown in Figure 30A and with the observation of the correlated result, a single check can be achieved upon the frame synchronization detection.

Figure 32 is a correlation processing apparatus for the downlink in accordance with a preferred embodiment of the present invention, in which the single check for each slot is executed upon the frame synchronization detection.

In this example, the symbol rate is 256,512,1024Ksps(N_{pilot} = 16), and the number of code sequences inputted for the frame synchronization detection is 8 in Figure 32. In other words, α = 8, so the code sequences C_1 to C_8 of Figure 21 are used. The column sequences, which are mapped with the branch stream of each channel I or Q of the first, third, fifth and seventh pilot symbols(symbol#1, symbol#3, symbol#5, and symbol#7) are utilized.

Thus, equation (27) is used without any transformation, and the characteristics of the frame synchronization words as indicated in equation (27) are utilized. As a result, the correlation processing apparatus of Figure 32 implements a single correlator for the frame synchronization detection.

Referring to Figure 32, a signal in one frame unit of the downlink dedicated physical control channel is received, and the demodulated column sequences of the symbol#1, symbol#3, symbol#5, and symbol#7 in the pilot pattern of Figure 24A are inputted in the order of the slot number.

The eight column sequences are inputted to a memory mapping/addressing block, in which the column sequences are stored in the frame unit and shifted and reversed by

using the cross-correlation between the frame synchronization words of equation (29). In this case, the column sequences stored in the frame unit are given by the following equation (33). At this time, the index (i, j) of each column sequence represents the memory address.

$$\hat{C}_1 = (\hat{C}_{1,0}, \hat{C}_{1,1},\ldots,\hat{C}_{1,14})$$

$$\hat{C}_2 = (\hat{C}_{2,0},\hat{C}_{2,1},\ldots,\hat{C}_{2,14})$$

$$\hat{C}_3 = (\hat{C}_{3,0},\hat{C}_{3,1},\ldots,\hat{C}_{3,14})$$

$$\hat{C}_4 = (\hat{C}_{4,0},\hat{C}_{4,1},\ldots,\hat{C}_{4,14})$$

$$\hat{C}_5 = (\hat{C}_{5,0},\hat{C}_{5,1},\ldots,\hat{C}_{5,14})$$

$$\hat{C}_6 = (\hat{C}_{6,0},\hat{C}_{6,1},\ldots,\hat{C}_{6,14})$$

$$\hat{C}_7 = (\hat{C}_{7,0},\hat{C}_{7,1},\ldots,\hat{C}_{7,14})$$

$$\hat{C}_8 = (\hat{C}_{8,0},\hat{C}_{8,1},\ldots,\hat{C}_{8,14}) \quad (33)$$

Each column sequence in the above equation (33) is shifted and reversed by the memory mapping/addressing block and then outputted. The outputs from the memory mapping/addressing block are added to provide the result value 'S2' as indicated by the following equation (34) to the correlator.

$$S2 = \hat{C}_{1'(j+\tau)(mod15)} - \hat{C}_{2'(j+\tau+7)(mod15)} + \hat{C}_{3'(-j-\tau+5)(mod15)} - \hat{C}_{4'(-j-\tau+12)(mod15)} + \hat{C}_{5'(j+\tau+10)(mod15)} - \hat{C}_{6'(j+\tau+2)(mod15)} + \hat{C}_{7'(-j-\tau)(mod15)} - \hat{C}_{8'(-j-\tau+7)(mod15)} \quad (34)$$

The correlator correlates the previously stored pilot sequence C_1 and the result value 'S2' of equation (34) to thereby detect the frame synchronization. At this time, the correlated result of Figure 33 and with the observation of the correlated result, a single check can be achieved upon the frame synchronization detection.

The correlation processing apparatus for the uplink and downlink channels according to the present invention adds the code sequences, while having different specific time delay and upward/downward ordering for each code sequence. Upon the addition of the code sequences, each sequence suffers from various kinds of channel characteristic to thereby obtain a time diversity effect.

In the case where the size of the code sequence stored is smaller than two frames, the continuity of the sequence by code sequences may be disconnected upon the correlation processing. However, the discontinuity of the sequence can provide the time diversity effect.

The number of the code sequences added is 2 or 3 or more, and in the case where the code sequences in the order of same direction(upward or downward direction) are

combined, the size of the memory can be reduced. In contrast, in the case where the code sequences in the order of different direction are combined, the time diversity can be obtained by the discontinuity of the sequence.

In the case where the code sequences where the time delay difference is small are combined, the size of the memory can be reduced. In contrast, in the case where the code sequences where the time delay difference is large are combined, the time diversity can be obtained.

As discussed above, a frame synchronization apparatus and method using an optimal pilot pattern according to the present invention can use a single correlator in the uplink or downlink, irrespective of the number of the code sequences used, to thereby render the hardware for the frame synchronization at the receiving side substantially simple.

In addition, the simplified hardware construction does not require any complicated software, so the frame synchronization can be detected in a simple manner.

The foregoing embodiments are merely exemplary and are not to be construed as limiting the present invention. The present teaching can be readily applied to other types of apparatuses. The description of the present invention is intended to be illustrative, and not to limit the scope of the claims. Many alternatives, modifications, and variations will be apparent to those skilled in the art. In the claims, means-plus-function clauses are

intended to cover the structures described herein as performing the recited function and not only structural equivalents but also equivalent structures.